Rewarding Learning

General Certificate of Secondary Education
2012

Technology and Design

Unit 2: Systems and Control
Element 1: Electronic and Microelectronic Control Systems

[GTD21]

TUESDAY 29 MAY, AFTERNOON

MARK SCHEME

General Marking Instructions

Introduction

Mark schemes are intended to ensure that the GCSE examinations are marked consistently and fairly. The mark schemes provide markers with an indication of the nature and range of candidates' responses. The mark schemes should be read in conjunction with these general marking instructions.

Assessment objectives

Below are the assessment objectives for GCSE Technology and Design.

Students must:

- recall select and communicate their knowledge and understanding of technology and design in a range of contexts (AO1);
- apply skills, knowledge and understanding, in a variety of contexts and in designing and making products (AO2); and
- analyse and evaluate products, including their design and production (AO3).

Flexibility in marking

Mark schemes are not intended to be totally prescriptive. No mark scheme can cover all the responses which candidates may produce. In the event of an unanticipated answer, examiners are expected to use their professional judgement to assess the validity of answers. If an answer is particularly problematic, then examiners should seek the guidance of the Supervising Examiner.

Positive Marking

Examiners are encouraged to be positive in their marking, giving appropriate credit for what candidates know, understand and can do rather than penalising candidates for errors or omissions. Examiners should make use of the whole of the available mark range for any particular question and be prepared to award full marks for a response which is as good as might reasonably be expected of a 16-year-old GCSe candidate

Awarding zero marks

Marks should only be awarded for valid responses and no marks should be awarded for an answer which is completely incorrect or inappropriate.

Types of mark schemes

Mark schemes for tasks or questions which require candidates to respond in extended written form are marked on the basis of levels of response which take account of the quality of written communication.

Other questions which require only short answers are marked on a point for point basis with marks awarded for each valid piece of information provided.

Levels of response
Tasks and questions requiring candidates to respond in extended writing are marked in terms of levels of response. In deciding which level of response to award, examiners should look for the "best-fit" bearing in mind that weakness in one area may be compensated for by strength in another. In deciding which mark within a particular level to award to any response, examiners are expected to use their professional judgement. The following guidance is provided to assist examiners.

- ***Threshold performance*:** Response which just merits inclusion in the level and should be awarded a mark at or near the bottom of the range.

- ***Intermediate Performance*:** Response which clearly merits inclusion in the level and should be awarded a mark at or near the middle of the range.

- ***High Performance*:** Response which fully satisfies the level description and should be awarded a mark at or near the top of the range.

Marking calculations
In marking answers involving calculations, examiners should apply the "own figure rule" so that candidates are not penalised more than once for a computational error.

Quality of written communication
Quality of written communication is taken into account in assessing candidates' responses to all tasks and questions that require them to respond in written form. These tasks and questions are marked on the basis of levels of response. The description for each level of response includes reference to the quality of written communication.

For conciseness, quality of written communication is distinguished within levels of response as follows:

Level 1: Quality of written communication is limited.
Level 2: Quality of written communication is satisfactory.
Level 3: Quality of written communication is very good.

In interpreting these level descriptions, examiners should refer to the more detailed guidance provided below:

Level 1 (Limited): The level of accuracy of presentation, spelling, punctuation and grammar is limited. The candidate makes a limited selection and use of an appropriate form and style of writing. The organisation of material may lack clarity and coherence. There is little use of specialist vocabulary.

Level 2 (Satisfactory): The level of accuracy of presentation, spelling, punctuation and grammar is satisfactory. The candidate makes a satisfactory selection and use of an appropriate form and style of writing supported with appropriate use of diagrams as required. Relevant material is organised with some clarity and coherence. There is some use of specialist vocabulary.

Level 3 (Very Good): The level of accuracy of presentation, spelling, punctuation and grammar is very good. The candidate successfully selects and uses the most appropriate form and style of writing, supported with precise and accurate use of diagrams where appropriate. Organisation of relevant material is very good. There is very good use of appropriate specialist vocabulary.

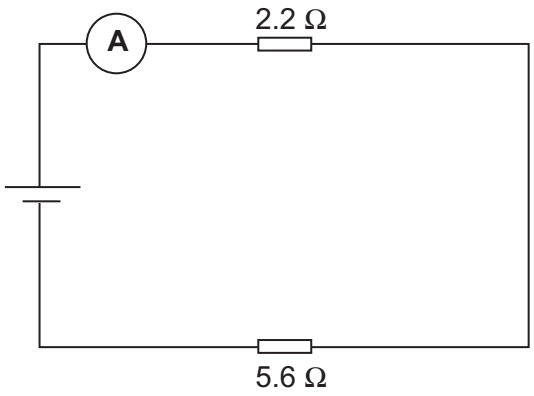
AVAILABLE MARKS

1 (a) (i) $V = I \times R$ **or**  **or current passing through a resistor is proportional to the voltage across it (or similar)** [3]

(ii) Total resistance = 2.2 + 5.6 = 7.8 Ω

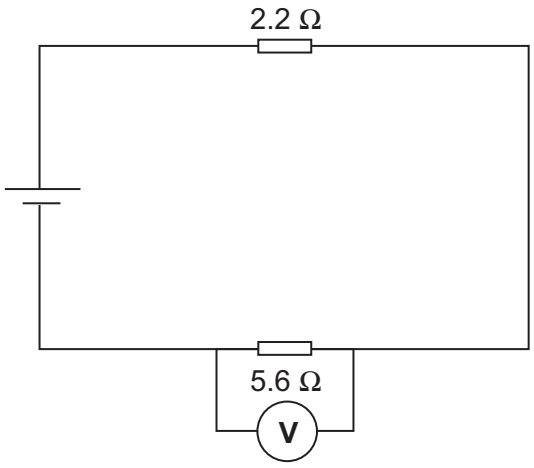
$$I = \frac{V}{R} = \frac{9}{7.8} = 1.154 \text{ A}$$ [4]

(iii)



[2]

(iv)



[2]

(v) $V = I \times R = 1.154 \times 5.6 = 6.46$ V
or Use ratios 5.6/7.8 of 9 which = 6.46 V [4]

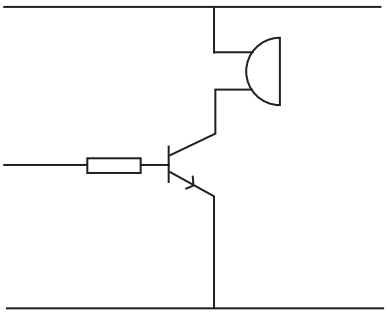
(b) (i) A = Relay coil
B = Relay make contact spring return [2]

(ii) Two functions:
An **electrical/electronic operated switch**

and **one** of the following **or** other suitable alternative

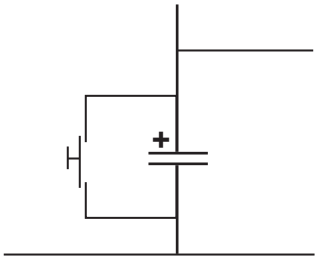
Enables **one circuit** to switch on a **separate** second circuit
Uses a small **control circuit to switch** a **much larger load current**
Control circuit **isolated** from **load circuit**
To switch circuits where **the output of the first** circuit **has insufficient power to drive the output device**
If DPDT can be used to **latch** a switching circuit [4]

			AVAILABLE MARKS
(c)	**(i)**	Potential Divider Circuit, Time Delay Circuit [1]	
	(ii)	A = Variable resistor [1] B = Polarised Capacitor [1]	
	(iii)	When S_1 is closed current travels from + to 0 rail through the variable resistor and the capacitor Capacitor charges up creating a time delay Capacitor resistance/voltage increases as it charges and when high enough Voltage increase and Current increase at point X. [3]	
(d)	**(i)**	Circuit as shown	



[1] for resistor correctly added
[2] for transistor correctly drawn and added
[2] for buzzer correctly drawn and added [5]

	(ii)	Current limiting resistor to protect the Transistor The transistor to function as an electronic switch [2]	
(e)	**(i)**	Addition as shown	



Correct symbol for Push to Make switch
Correct connections/location [2]

	(ii)	It will re-set the circuit by Opening S_1 and pressing the Push to Make switch Capacitor will then discharge Buzzer will switch off until S_1 is closed and capacitor fills (4 × [1]) [4]	40

AVAILABLE MARKS

2 **(a)** **(i)** 3 Bit Pattern [4]

0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

(ii) 00110010 [2]

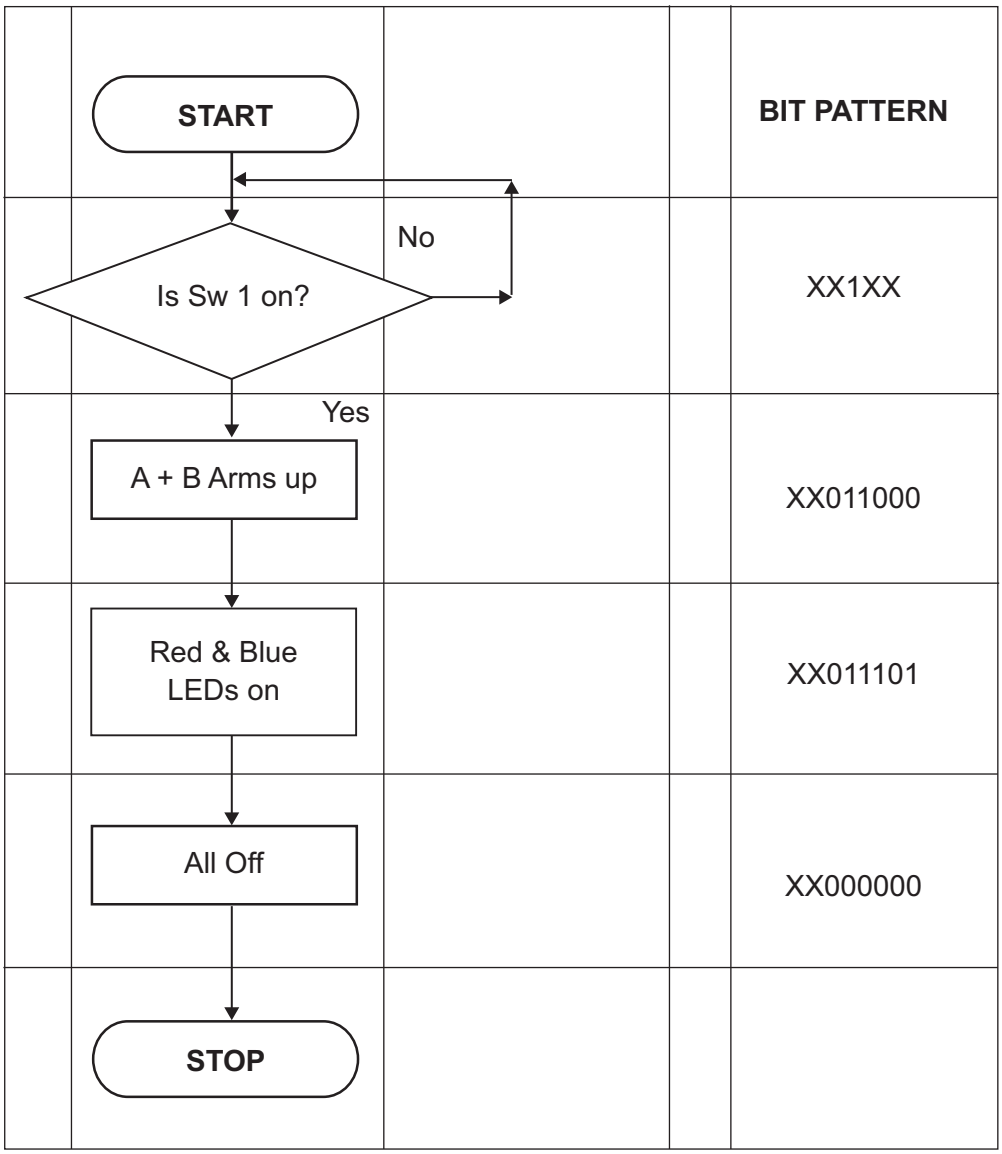
(iii) 28 [2]

(iv) Higher current output devices cannot be switched directly by the PIC microcontroller chip, or they require a transistor switching circuit [2]

(v) Devices: Bulbs; Motor [2]

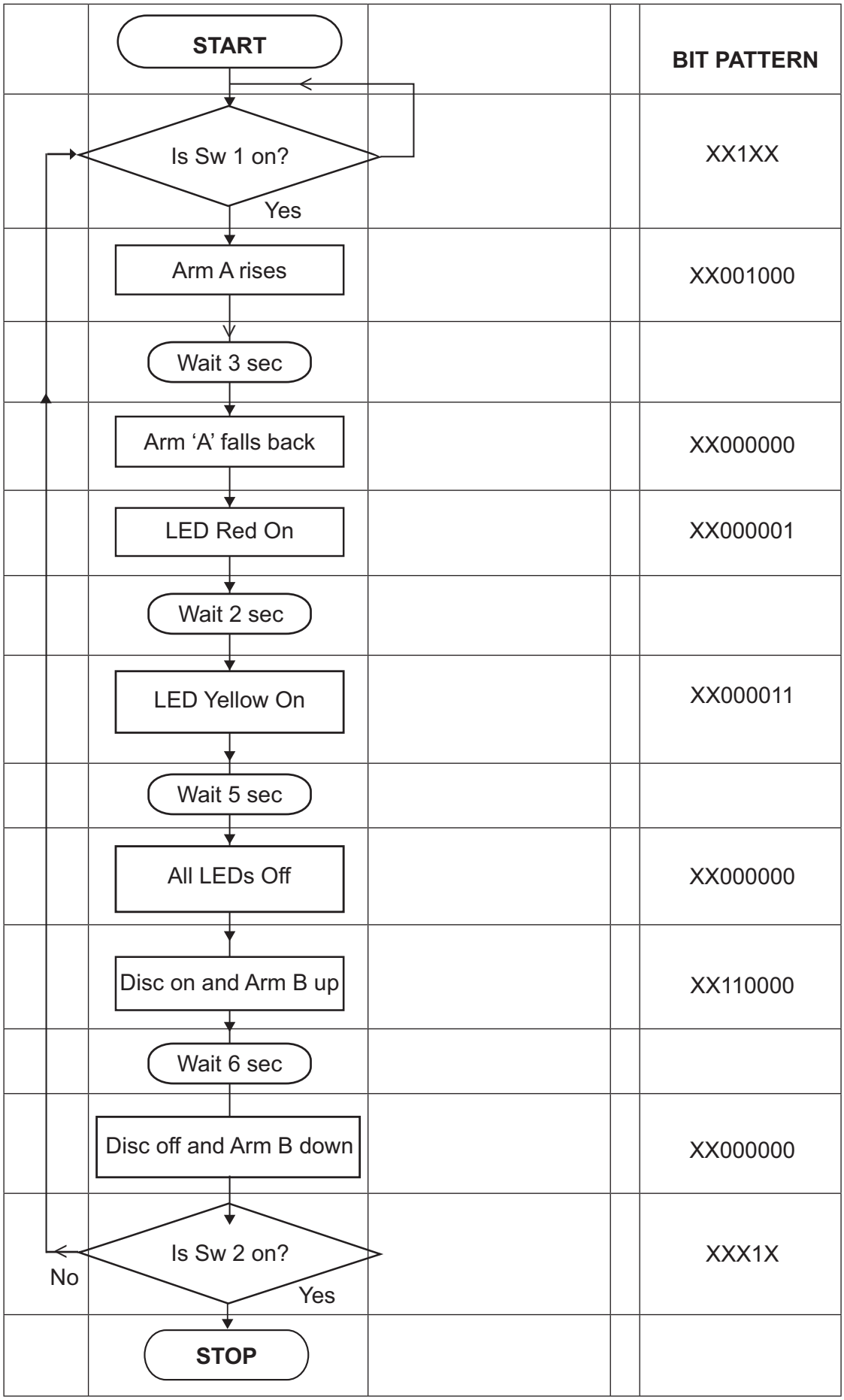
(b) (i)

AVAILABLE MARKS



[10]

(b) (ii)



[18]

Total

AVAILABLE MARKS

40

80