



*Rewarding Learning*

**General Certificate of Secondary Education  
2017**

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## **Technology and Design**

Unit 2: Systems and Control  
Element 1: Electronic and Microelectronic  
Control Systems

**[GTD21]**

**THURSDAY 8 JUNE, AFTERNOON**

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# **MARK SCHEME**

## General Marking Instructions

### **Introduction**

Mark schemes are intended to ensure that the GCSE examinations are marked consistently and fairly. The mark schemes provide markers with an indication of the nature and range of candidates' responses. The mark schemes should be read in conjunction with these general marking instructions.

### **Assessment objectives**

Below are the assessment objectives for GCSE Technology and Design.

Students must:

- recall select and communicate their knowledge and understanding of technology and design in a range of contexts (AO1);
- apply skills, knowledge and understanding, in a variety of contexts and in designing and making products (AO2); and
- analyse and evaluate products, including their design and production (AO3).

### **Flexibility in marking**

Mark schemes are not intended to be totally prescriptive. No mark scheme can cover all the responses which candidates may produce. In the event of an unanticipated answer, examiners are expected to use their professional judgement to assess the validity of answers. If an answer is particularly problematic, then examiners should seek the guidance of the Supervising Examiner.

### **Positive Marking**

Examiners are encouraged to be positive in their marking, giving appropriate credit for what candidates know, understand and can do rather than penalising candidates for errors or omissions. Examiners should make use of the whole of the available mark range for any particular question and be prepared to award full marks for a response which is as good as might reasonably be expected of a 16-year-old GCSE candidate.

### **Awarding zero marks**

Marks should only be awarded for valid responses and no marks should be awarded for an answer which is completely incorrect or inappropriate.

### **Types of mark schemes**

Mark schemes for tasks or questions which require candidates to respond in extended written form are marked on the basis of levels of response which take account of the quality of written communication.

Other questions which require only short answers are marked on a point for point basis with marks awarded for each valid piece of information provided.

**Levels of response**

Tasks and questions requiring candidates to respond in extended writing are marked in terms of levels of response. In deciding which level of response to award, examiners should look for the “best-fit” bearing in mind that weakness in one area may be compensated for by strength in another. In deciding which mark within a particular level to award to any response, examiners are expected to use their professional judgement. The following guidance is provided to assist examiners.

- **Threshold performance:** Response which just merits inclusion in the level and should be awarded a mark at or near the bottom of the range.
- **Intermediate Performance:** Response which clearly merits inclusion in the level and should be awarded a mark at or near the middle of the range.
- **High Performance:** Response which fully satisfies the level description and should be awarded a mark at or near the top of the range.

**Marking calculations**

In marking answers involving calculations, examiners should apply the “own figure rule” so that candidates are not penalised more than once for a computational error.

**Quality of written communication**

Quality of written communication is taken into account in assessing candidates’ responses to all tasks and questions that require them to respond in written form. These tasks and questions are marked on the basis of levels of response. The description for each level of response includes reference to the quality of written communication.

For conciseness, quality of written communication is distinguished within levels of response as follows:

Level 1: Quality of written communication is limited.

Level 2: Quality of written communication is satisfactory.

Level 3: Quality of written communication is very good.

In interpreting these level descriptions, examiners should refer to the more detailed guidance provided below:

**Level 1 (Limited):** The level of accuracy of presentation, spelling, punctuation and grammar is limited. The candidate makes a limited selection and use of an appropriate form and style of writing. The organisation of material may lack clarity and coherence. There is little use of specialist vocabulary.

**Level 2 (Satisfactory):** The level of accuracy of presentation, spelling, punctuation and grammar is satisfactory. The candidate makes a satisfactory selection and use of an appropriate form and style of writing supported with appropriate use of diagrams as required. Relevant material is organised with some clarity and coherence. There is some use of specialist vocabulary.

**Level 3 (Very Good):** The level of accuracy of presentation, spelling, punctuation and grammar is very good. The candidate successfully selects and uses the most appropriate form and style of writing, supported with precise and accurate use of diagrams where appropriate. Organisation of relevant material is very good. There is very good use of appropriate specialist vocabulary.

Answer **all** questionsAVAILABLE  
MARKS

- 1 (a) (i) Resistance  
Ohms  
Current  
Amps

[1]  
[1]  
[1]  
[1]

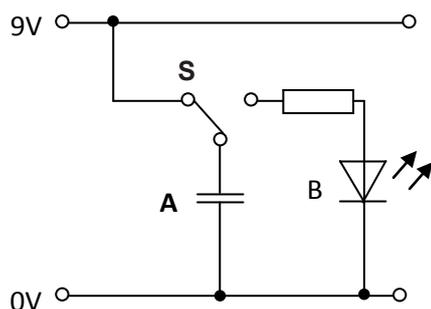
(ii)  $RT = \frac{R1 \times R2}{R1 + R2} = \frac{2.7 \times 6.8}{2.7 + 6.8} = \frac{18.36}{9.5} = 1.93\Omega$

[2]

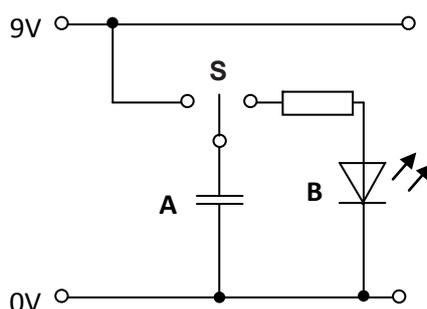
$I = V/R = 5/1.93 = 2.6A$

[2]

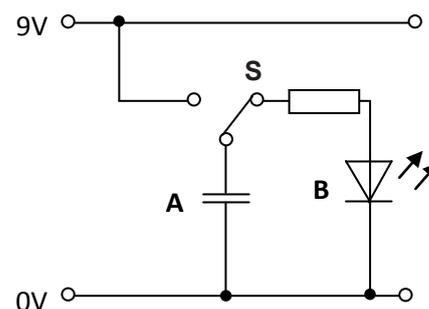
(b)



(x)



(y)



(z)

- (i) **A** = Capacitor  
**B** = Light emitting diode (LED)

[1]  
[1]

- (ii) Position **(x)**: Switch connects 9V rail to 0V rail through the capacitor. Current flow charges up capacitor and when full no more current will flow.

[2]

Position **(y)**: Capacitor is isolated. It will stay charged but will slowly leak its charge if left in this position.

[2]

Position **(z)**: Switch connects capacitor to the LED and 0V rail. LED will light brightly at first then dim and go out as capacitor discharges.

[2]

- (iii) Component **A** will be unable to discharge through component **B**.  
Component **B** will only operate when connected to the 9V rail.

[1]

[1]

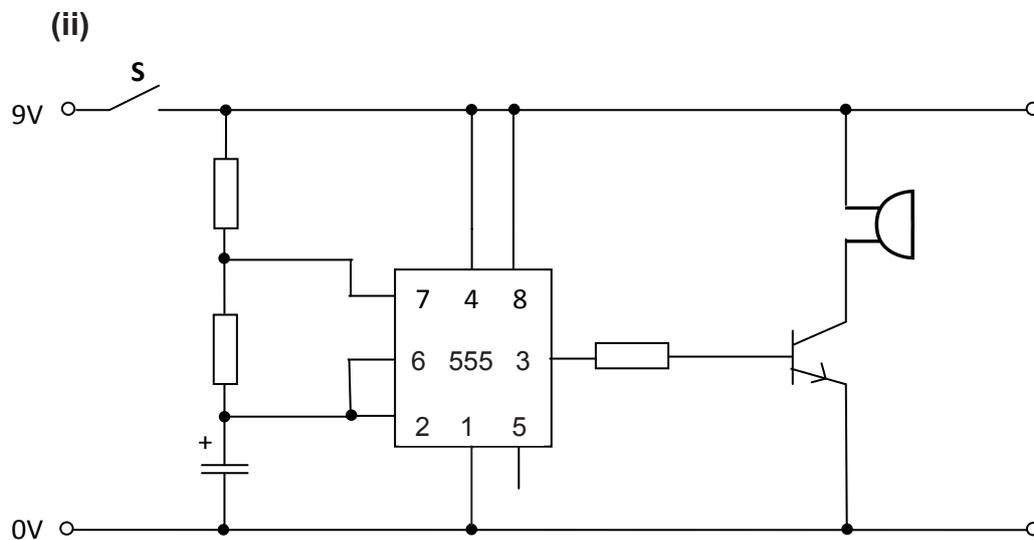
All valid responses will be considered.

(c) (i) They produce a Time delay at X or they form a Voltage Divider/Potential divider circuit. [1]

(ii)  $T = R \times C$   $T = R \times C$   
 $T = 120\text{k}\Omega \times 100\mu\text{F}$  OR  $T = 120,000 \times 0.0001$   
 $T = 12000\text{ms}$   $T = 12 \text{ secs.}$  [3]

(iii) Reduce the value of R [2]  
 Reduce the value of C

(d) (i) A monostable circuit output is either on or off/has one stable state  
 An astable circuit output turns on and off continuously/has no stable state.  
 Or suitable alternative answers [2]



Pins 6 and 2 tied. [2]  
 Pins 2 and 7 connected as shown. [2]  
 Pins 4, 8 and 1 as shown. [3]  
 Buzzer correctly drawn and inserted. [1]  
 Transistor correctly drawn and inserted. [1]  
 Protective resistor in correct place. [1]  
 Pin 3 connected. [1]  
 Top and bottom rails correct for buzzer and transistor. [1] [12]

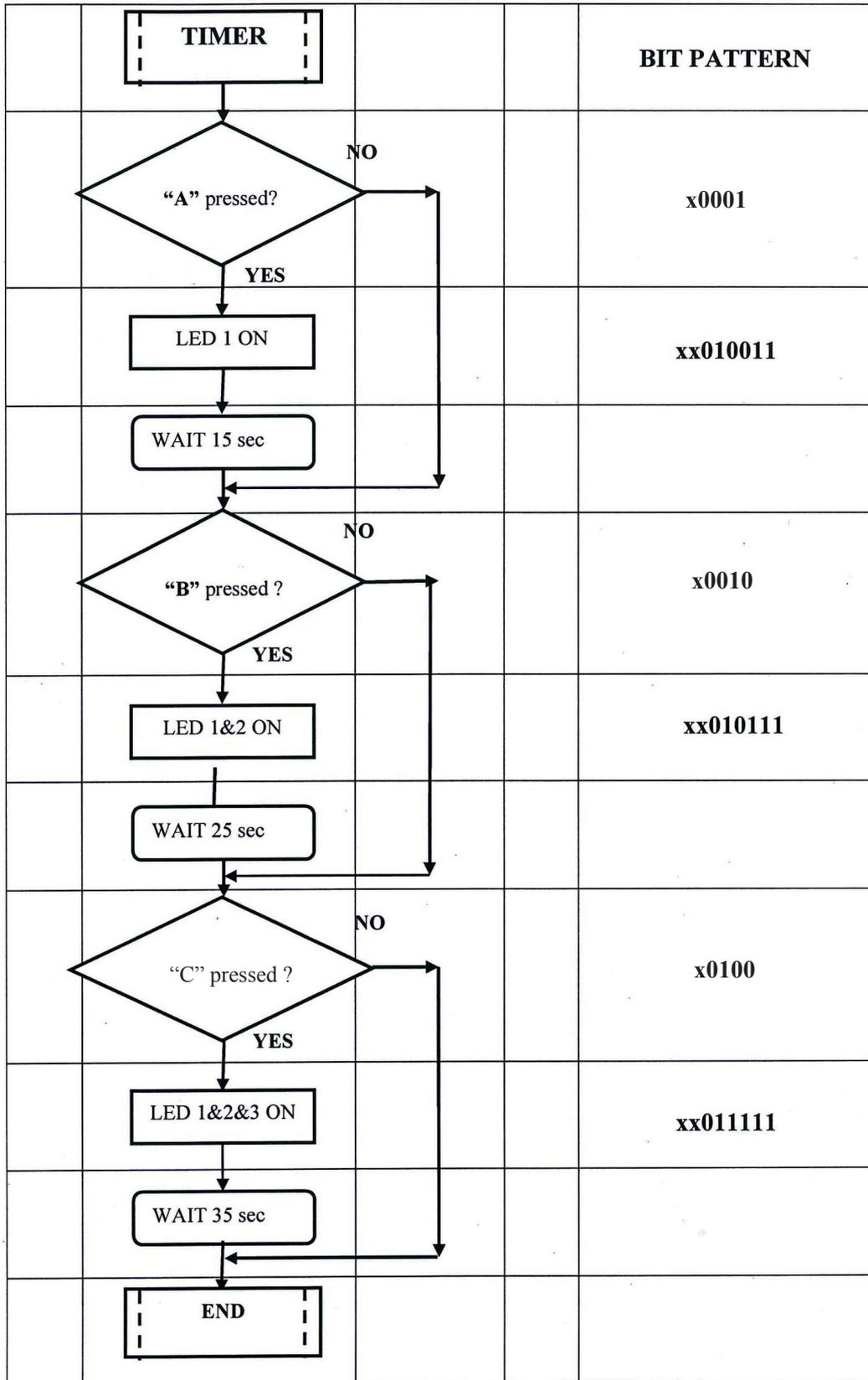
(iii) The buzzer will sound on and off continuously. [2]

40

- 2 (a) (i) PIC requires fewer external components  
 PIC allows greater flexibility and can be programmed to change its function  
 PIC has more outputs  
 PIC can reduce the size of a circuit  
 PIC are more easily adjusted for complex sequences  
 PIC has a wider range of applications  
 Any **two**  
 (2 × [1]) [2]
- (ii) PIC is more expensive than 555 IC chips  
 It is necessary to program a PIC  
 Any **one** [1]
- (iii) Decimal number = 29 [2]
- (iv) Binary number 0101111 [2]
- (v)
- |   |   |   |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 1 |
- (5 × [1]) [5]

AVAILABLE  
MARKS

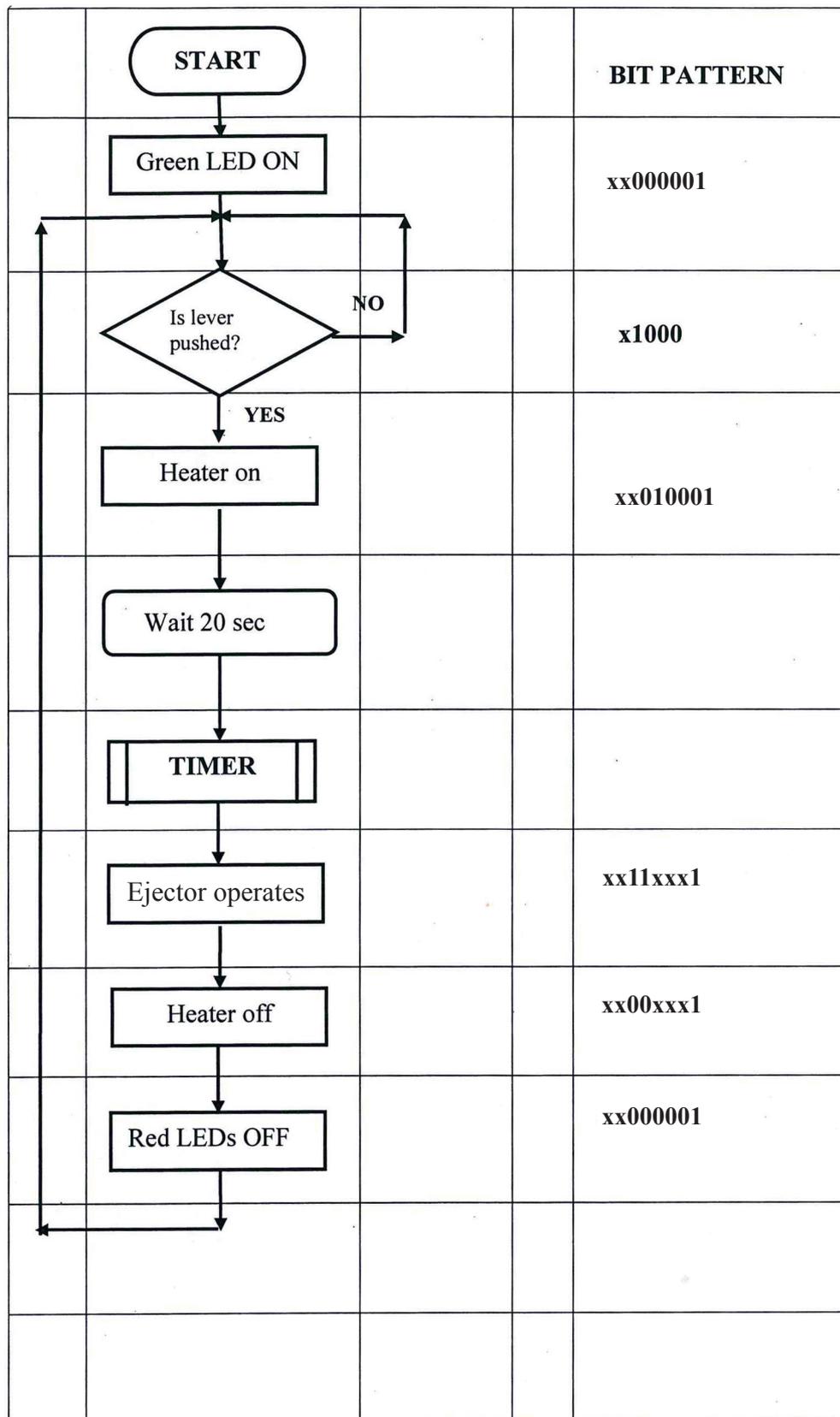
(b) (i)



[13]

AVAILABLE MARKS

(b) (ii)



[15]

**Total**

AVAILABLE MARKS

40

80