



**GCE**

**Electronics**

Unit **F615**: Communications Systems

Advanced GCE

**Mark Scheme for June 2015**

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All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

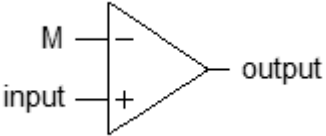
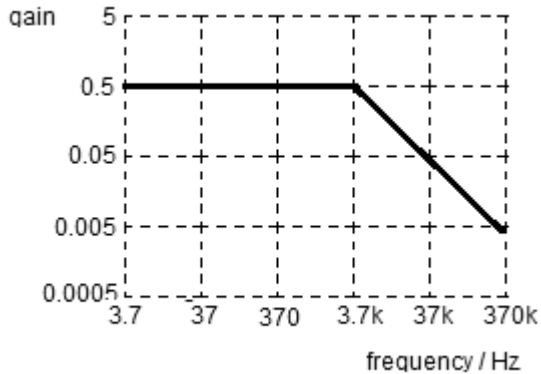
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Question			Answer	Mark	Guidance
1	a	i	set intensity / brightness; of each pixel; one after the other / from left to right in successive rows / from top to bottom (on the screen);	1 1 1 1	<b>ignore</b> raster scan
		ii	as each pulse arrives; start to scan a new row of pixels;	1 1	<b>not just</b> new line
		pixels per second = $320 / 80\mu = 4.0 \times 10^6$ ; bandwidth = 2.0 MHz;	1 1	<b>no ecf</b> for incorrect pixel rate	
	iii iv	frame display time = $220 \times 80\mu = 17.6$ ms; refresh rate = 57 Hz; greater than 25 Hz; so image is flicker-free;	1 1 1 1	<b>accept</b> range of 20 to 30 Hz <b>ecf</b> from calculated refresh rate if less than 25 Hz	
	b	two more cables needed; allows separate video signals (for three pixels in a cluster); for red, green and blue pixels;	1 1 1	<b>ignore</b> RGB	
2	a		3	correct sinusoidal shape with constant amplitude [1] correct amplitude [1] correct period [1]  <b>accept</b> any phase	

Question		Answer	Mark	Guidance
	b	Z; Y; 113; X	2	113 kHz for [1] X, Y and Z correct for [1] <b>accept</b> X and Y interchanged
	c	i	break frequency from 5 kHz to 10 kHz; $f_0 = \frac{1}{2\pi RC}$ ; use of C between 50 pF and 100 pF;	1 1 1 <b>no ecf</b> for incorrect break frequency
		ii	<b>transfer characteristic</b> <ul style="list-style-type: none"> <li>• diode only conducts in forward bias;</li> <li>• with voltage drop;</li> <li>• which rises steeply with increasing current;</li> </ul> <b>circuit operation</b> <ul style="list-style-type: none"> <li>• only <u>negative</u> parts of signal amplified;</li> <li>• carrier frequency filtered out by capacitor and (feedback) resistor</li> </ul>	1 1 1 1 1 <b>accept</b> any value below 1 V  <b>look for</b> high quality responses to circuit operation  <b>accept</b> (rectified) signal smoothed by capacitor and resistor <b>accept</b> treble cut filter as capacitor and feedback resistor <b>ignore</b> references to gain
<b>3</b>	a	output has a frequency of 27.2 MHz (for zero volt signal); frequency increases/decreases with increasing signal voltage; amplitude of output remains constant;	1 1 1	<b>ignore</b> amplitude
	b	bandwidth = 200 kHz maximum frequency = 40 kHz	1 1	<b>no ecf</b> on incorrect bandwidth
	c	removes noise / interference added to FM signal; by restoring FM signal to a square wave / digital signal;	1 1	
	d	output of monostable is a fixed duration pulse; for each cycle/pulse of FM carrier; so mean voltage of monostable output changes for changing frequency of FM carrier; (treble cut) filter removes carrier frequencies; smoothing / averaging the pulses (producing a copy of the original signal);	1 1 1 1 1	<b>accept</b> rising / falling edge for cycle <b>accept</b> pulse spacing depends on frequency of carrier

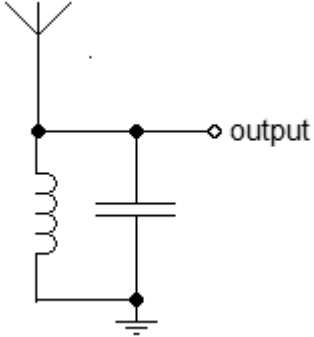
Question		Answer	Mark	Guidance	
4	a	<p><b>ST threshold calculation</b></p> <ul style="list-style-type: none"> <li><math>I = 13/42k = 3.09 \times 10^{-4} \text{ A};</math></li> <li><math>V = 3.09 \times 10^{-4} \times 27k = 8.4 \text{ V};</math></li> </ul> <p><b>RG calculation</b></p> <ul style="list-style-type: none"> <li><math>\frac{4 \times 8.4}{T} = \frac{13}{15k \times 3.3n}</math></li> <li><math>T = 1.3 \times 10^{-4} \text{ s, so } f = 7.8 \text{ kHz};</math></li> </ul>	1 1  1 1	method shown [1] <b>accept</b> $13 \times (27/42)$ <b>not</b> $13 \times (-27/42)$ correct value [1]  method shown [1]  correct value [1] <b>accept</b> anything that rounds to 8 kHz with correct method for [2]	
	b	i		2	comparator with any input to M [1] correct input and output labels [1]
		ii	voltage at input; sets mark-space ratio of output;	1 1 <b>ignore</b> amplitude / signal <b>ignore</b> frequency <b>ignore</b> description of op-amp behaviour	
	c	i		5	$G = -\frac{R_f}{R_{in}}$ use of $\frac{R_f}{R_{in}}$ to calculate low frequency gain of (-) 0.51 [1]  $f_0 = \frac{1}{2\pi RC}$ use of $\frac{1}{2\pi RC}$ to calculate break frequency of 3.7 kHz [1] suitable log axes labelled [1] correct shape [1] correct break frequency [1]  <b>accept</b> 4, 40, 400 ... as frequency axis labels
		ii	break frequency is close to maximum signal frequency that can be correctly coded; need at least two samples per signal cycle; maximum signal frequency should be $7.8 / 2 = 3.9 \text{ kHz};$	1 1 1	

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Question		Answer	Mark	Guidance
5	a	Any of the following for [1]; <ul style="list-style-type: none"> <li>• put metal shielding around cables</li> <li>• keep cables away from other systems</li> <li>• keep cables short</li> </ul> idea that interference is signal from other circuits;	1  1	<b>accept</b> use optical fibre [1] as cladding stops outside signals [1]  <b>accept</b> use frequency / digital coding [1] as interference can be removed by ST (at receiver) [1]
	b	any <b>two</b> of the following: <ul style="list-style-type: none"> <li>• both cables follow same path</li> <li>• pick up the same interference</li> <li>• so can be removed by difference amplifier</li> </ul>	2	<b>not</b> noise
	c	signal at A is copied to C by voltage follower; signal at A is inverted and placed at B; signals arrive at D and E with interference; difference amplifier cancels out interference; and recreates (double) the original signal (at F);	1 1 1 1 1	
6	a	each station is allocated a channel / carrier frequency; with a unique range of frequencies / bandwidth;	1 1	<b>allow</b> frequency for carrier
	b	i	channel bandwidth = 9 kHz; channels = $(1607 - 527) / 9 = 120$	1 1 <b>ecf</b> 4.5 kHz gives 240 channels for [1]
		ii	much larger bandwidth per channel; so fewer channels / stations in the band;	1 1
	iii	EITHER FM (receivers) can eliminate noise; by using limiters / Schmitt triggers; to restore shape of signal; OR AM (receivers) can't eliminate noise; because it affects amplitude; so can't be separated from signal by demodulator;	1 1 1	<b>accept</b> interference for noise, <b>accept</b> less susceptible to noise

Question		Answer	Mark	Guidance
7	a		5	<p>correct arrangement of components [1]</p> <p><b>ignore</b> resistor in series with aerial</p> <p>earthing / 0 V shown <u>and</u> output labelled [1]</p> <p><math>LC = 1.9 \times 10^{-15} \text{ s}</math> [1]</p> <p>C in range 1 pF to 1 <math>\mu\text{F}</math> [1]</p> <p>use of <math>f_0 = \frac{1}{2\pi\sqrt{LC}}</math> to justify correct values [1]</p>
	b	i	filter centre frequency 470 kHz; oscillator = 3650 + 470 = 4120 kHz;	1 1 <b>accept</b> 3180 kHz for [2] <b>accept</b> 4100, 4140, 3200 or 3160 kHz for [1]
		ii	any four of the following: <ul style="list-style-type: none"> <li>oscillator produces signal of one frequency;</li> <li>which is at carrier <math>\pm</math> filter frequency;</li> <li>which amplitude modulates tuner signal in mixer;</li> <li>to produce a copy of tuner signal;</li> <li>which can pass through filter;</li> </ul>	4  <b>not</b> mixes / combines <b>accept</b> create sidebands
	c	i	amplifier; boosts signals from weak transmitter;	1 1 <b>accept</b> aerial [1] altering position / length increases signal from weak stations [1].
		ii	filter; only lets through carrier and sidebands from one transmitter;	1 1 <b>not</b> tuned circuit
8	a	i	takes (serial) bits from link one after the other; assembles them into (parallel) words;	1 1 <b>allow just</b> serial-to-parallel converter for [1]
		ii	takes in binary words; outputs corresponding voltage;	1 1 <b>allow just</b> digital-to-analogue converter for [1]
	b	i	number of states = $4/0.025 = 160$ ; $2^7 = 128$ , $2^8 = 256$ ; so needs 8 bits;	1 1 1 <b>accept</b> $\log_2 160 = 7.32$ correct answer with no working for [1]
		ii	must sample twice in each cycle; sample frequency = $1/125\mu = 8 \text{ kHz}$ ; maximum signal frequency = 4 kHz;	1 1 1

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Question		Answer	Mark	Guidance
	c i	any five of the following; <ul style="list-style-type: none"> <li>• pulse sets flip-flop</li> <li>• makes register load word from input</li> <li>• AND gate with one input high outputs pulses</li> <li>• clock pulses appear at CK</li> <li>• contents of register / bits appear at output in turn</li> <li>• counter output increases on each clock pulse</li> <li>• logic system resets flip-flop and counter at end</li> </ul>	5	
	ii	need one for each bit of the word at input; one for the start bit (before the word); one for the stop bit (at the end of the word);	1 1 1	
		Total	107	
		QWC	3	Overleaf
		=	110	



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