OCR
Oxford Cambridge and RSA

Thursday 25 May 2017 – Afternoon

AS GCE ELECTRONICS

F612/01 Signal Processors

Candidates answer on the Question Paper.

OCR supplied materials:
None

Other materials required:
- Scientific calculator

Duration: 1 hour 30 minutes

Candidate forename		Candidate surname	

Centre number						Candidate number				

INSTRUCTIONS TO CANDIDATES

- Write your name, centre number and candidate number in the boxes above. Please write clearly and in capital letters.
- Use black ink. HB pencil may be used for graphs and diagrams only.
- Answer **all** the questions.
- Read each question carefully. Make sure you know what you have to do before starting your answer.
- Write your answer to each question in the space provided. If additional space is required, you should use the lined page(s) at the end of this booklet. The question number(s) must be clearly shown.
- Do **not** write in the barcodes.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **90**.
- You will be awarded marks for your Quality of Written Communication.
- You are advised to show all the steps in any calculations.
- This document consists of **16** pages. Any blank pages are indicated.

A scientific calculator may be used for this paper

Data Sheet

symbol	meaning
start	start the program
a a	link to part of the program with the same label a
stop	stop the program
let Sn=b	place the byte b in register Sn
let Sn=Sn+b	add the byte b to the byte in register Sn
let Sn=Sm	copy the byte in register Sm into register Sn
let Sn=Sn–b	subtract the byte b from the byte in register Sn
pause t	introduce a time delay of t milliseconds
Sn=b (yes / no)	branch if the byte in register Sn is equal to the byte b
Sn>b (yes / no)	branch if the byte in register Sn is greater than the byte b
let Sn=input	copy the byte at the input port to register Sn
let output=Sn	copy the byte in register Sn to the output port
read adc,S0	activate the analogue-to-digital converter and store the result in register S0

Data Sheet

Unless otherwise indicated, you can assume that:

- op-amps are run off supply rails at +15 V and –15 V
- logic circuits are run off supply rails at +5 V and 0 V.

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7\,RC$
relaxation oscillator period	$T = 0.5\,RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{out} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_d}$
inverting amplifier gain	$G = -\frac{R_f}{R_{in}}$
summing amplifier	$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$
break frequency	$f_0 = \frac{1}{2\pi RC}$
Boolean Algebra	$A.\overline{A} = 0$
	$A + \overline{A} = 1$
	$A.(B + C) = A.B + A.C$
	$\overline{A.B} = \overline{A} + \overline{B}$
	$\overline{A + B} = \overline{A}.\overline{B}$
	$A + A.B = A$
	$A.B + \overline{A}.C = A.B + \overline{A}.C + B.C$

Answer **all** the questions.

1 Fig. 1.1 is a block diagram for a NAND gate bistable.

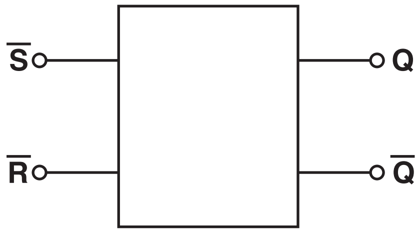

Fig. 1.1

(a) The bistable has two active-low inputs (**$\overline{S}$** and **$\overline{R}$**) and two outputs (**Q** and **$\overline{Q}$**).

(i) Complete the truth table to show how the signals at the inputs can be used to set, reset and not change the signals at the outputs.

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
		1	
			1
		no change	no change

[3]

(ii) Complete the truth table for a single NAND gate.

B	A	Q

[2]

(iii) Draw in the space below to show how NAND gates can be connected to make the bistable of Fig. 1.1. Label all inputs and outputs.

[3]

(b) By adding other logic gates, a NAND-gate bistable can be made into a latch or a D flip-flop. Each of these circuits has three terminals, labelled as follows:

- clock
- input D
- output Q

Describe the **difference** between the behaviour of a latch and a D flip-flop.

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.... **[2]**

2 Fig. 2.1 shows an op-amp arranged as an amplifier.

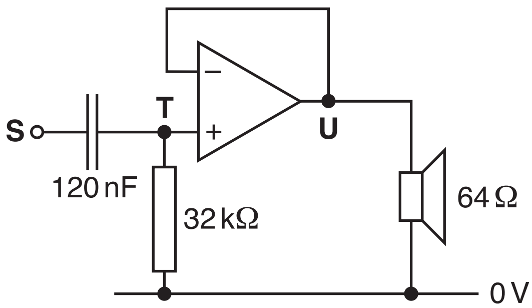

Fig. 2.1

(a) The amplifier contains a filter between **S** and **T**.

(i) Show that the break frequency of the filter is about 40 Hz.

[2]

(ii) Draw on the axes of Fig. 2.2 to show how the gain of the filter between **S** and **T** depends on the frequency of the signal.

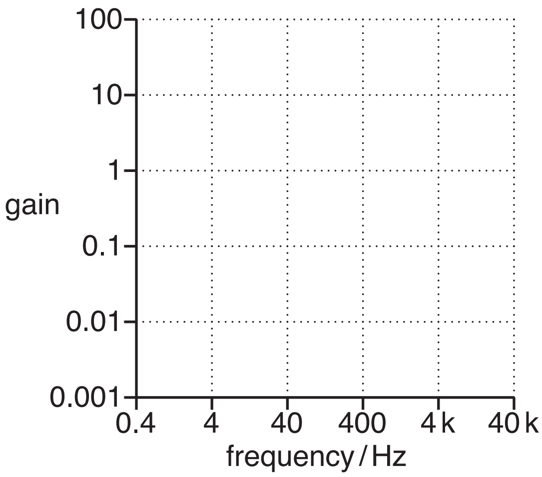

Fig. 2.2

[2]

(iii) By considering the impedance of the resistor and capacitor, explain the shape of the graph that you have drawn in Fig. 2.2.

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.... **[3]**

(b) **(i)** State a value for the voltage gain of the amplifier between **T** and **U** in Fig. 2.1.

voltage gain = ... **[1]**

(ii) Explain your answer to **(b)(i)** by referring to the transfer characteristics of the op-amp.

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.... **[2]**

(c) The circuit of Fig. 2.1 is part of an audio system.

Explain its functions in an audio system.

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.... **[3]**

3 Fig. 3.1 shows a D flip-flop arranged as a one-bit counter.

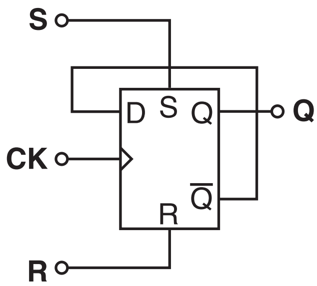

Fig. 3.1

(a) (i) Complete the timing diagram of Fig. 3.2 to show the behaviour of the circuit shown in Fig. 3.1.

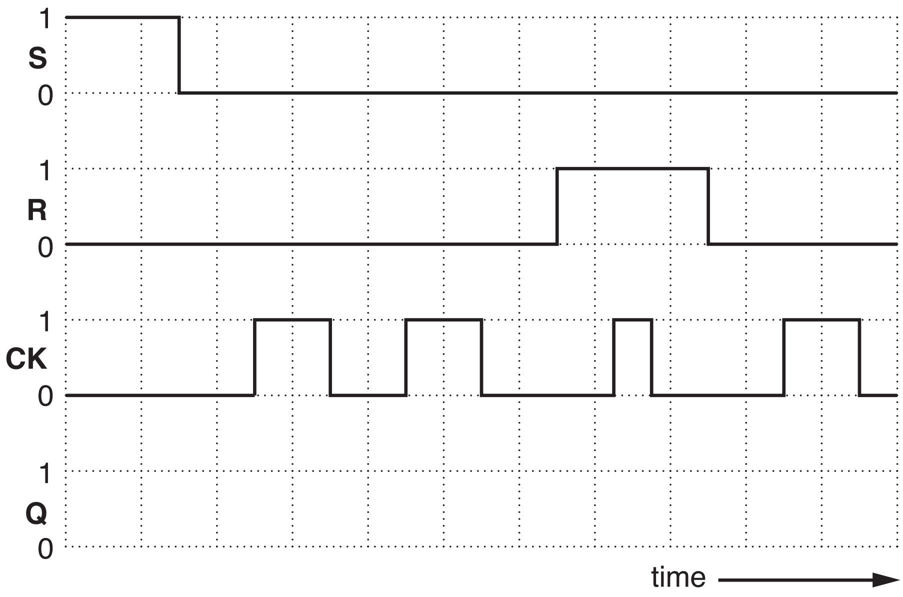

Fig. 3.2

[3]

(ii) Use the properties of a D flip-flop to explain how **CK** affects the state of **Q** in Fig. 3.1 when **S** and **R** are low.

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.... **[3]**

(b) The circuit of Fig. 3.3 contains three one-bit counters.

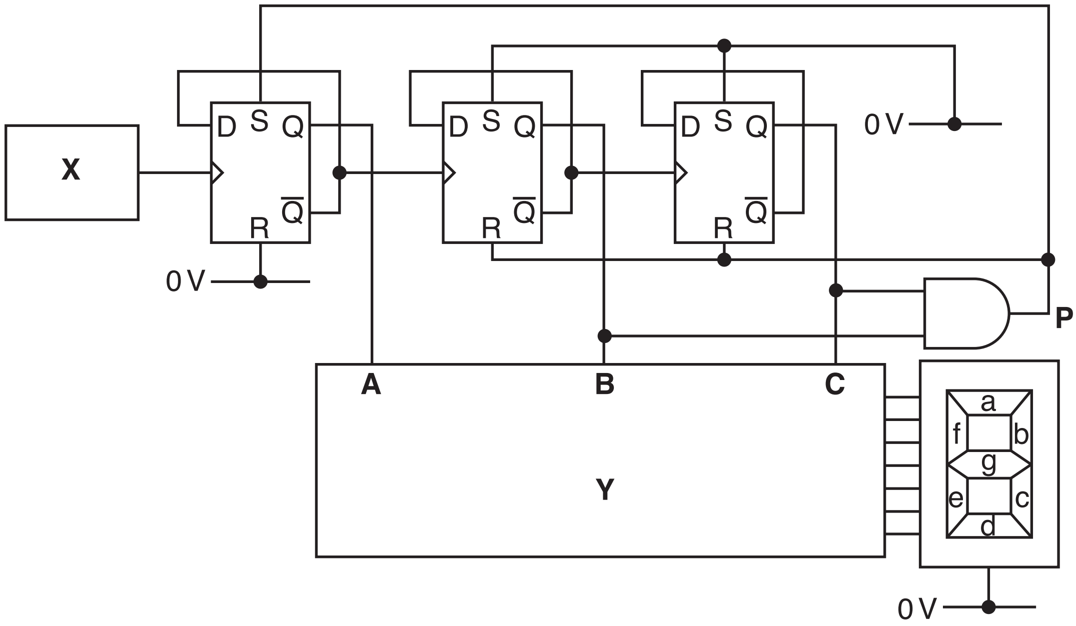

Fig. 3.3

The seven segment display shows a continuous sequence of numbers, changing at half second intervals.

(i) Describe the output of the block marked **X** in Fig. 3.3.

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.... **[2]**

(ii) Name the block marked **Y** in Fig. 3.3.

.... **[1]**

(iii) State and explain the sequence of numbers shown on the display several seconds after the circuit has been switched on.

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.... **[5]**

4 Fig. 4.1 shows a microcontroller system which can be used to test reaction times.

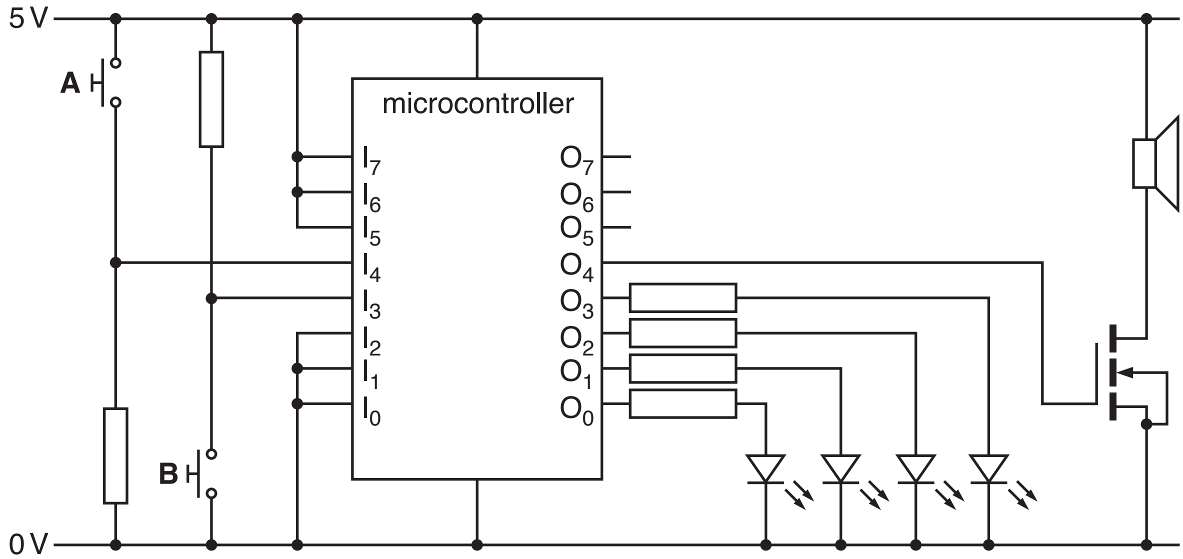

Fig. 4.1

Here are the instructions for use

- press and release switch **A**
- wait until the LEDs glow
- press switch **B** as soon as possible
- if any LEDs are still glowing, your reaction time is good

(a) Complete the table to show the words at the input port for two input conditions.

Switch(es) pressed	Binary	Hexadecimal
		E8
	11110000	

[2]

(b) The incomplete flowchart of Fig. 4.2 is for the first part of the program. It passes control to **a** when only switch **A** has been pressed. Complete the flowchart.

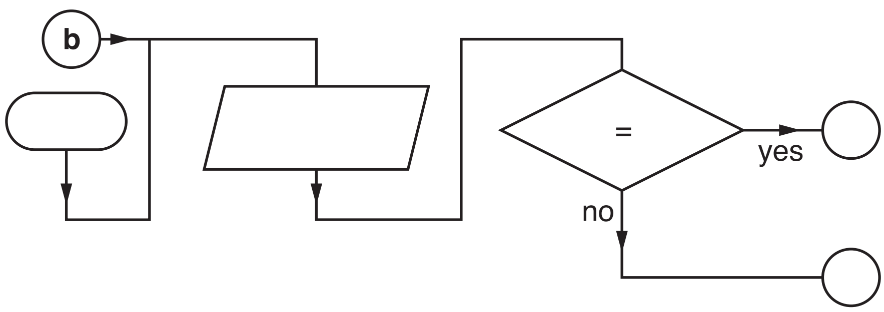

Fig. 4.2

[4]

(c) Fig. 4.3 shows the flowchart for the next part of the program.

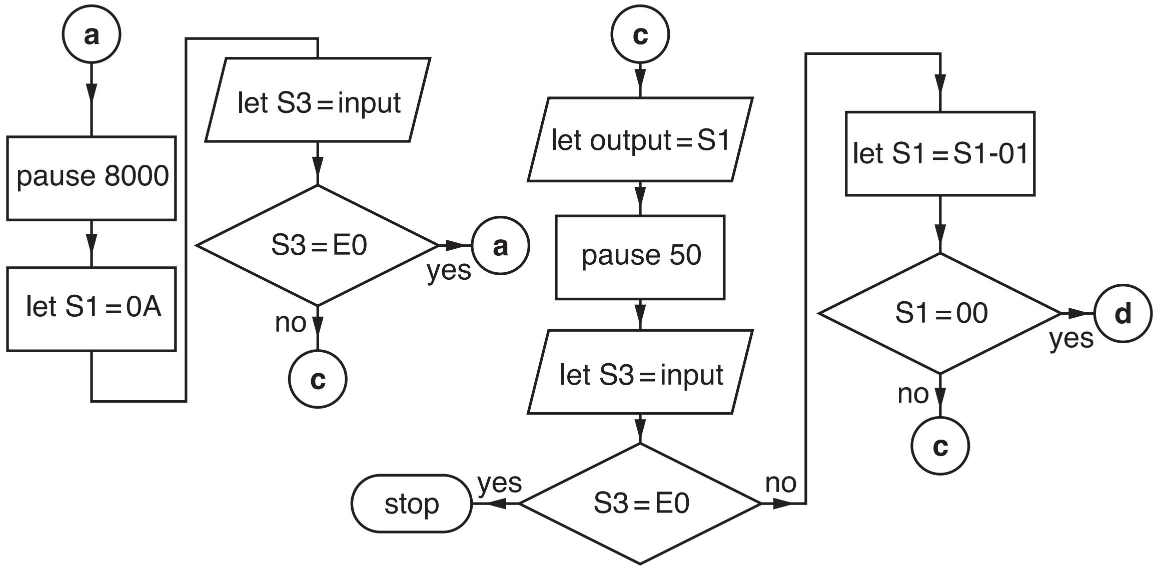

Fig. 4.3

Explain the effect that this part of the program has on the outputs of the system.

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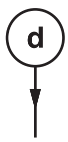
.... **[7]**

(d) The final part of the program feeds a square wave of frequency 250 Hz into the gate of the MOSFET, with all the LEDs on. Complete the flowchart below.



[5]

5 An audio system contains a tone control with the gain-frequency graph shown in Fig. 5.1.

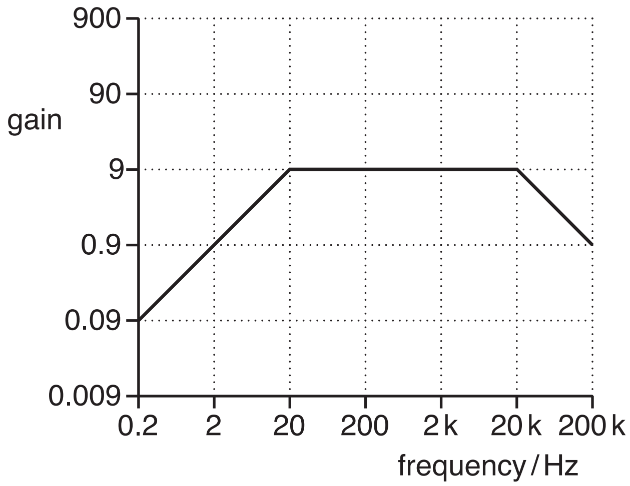


Fig. 5.1

(a) The tone control contains two active filters based on op-amps.
Complete the circuit of Fig. 5.2 to show how the tone control can be built.
Show all labels and component values, and justify them with calculations.

Fig. 5.2

[8]

(b) Fig. 5.3 is a block diagram for the complete audio system.

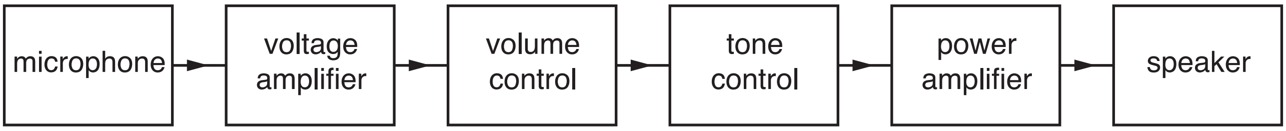


Fig. 5.3

(i) The voltage amplifier has a gain of +100 and an input impedance of 47 kΩ.
Complete the circuit of Fig. 5.4 for the voltage amplifier.
Show all component values and justify them with calculations.

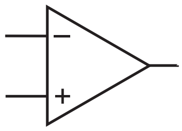


Fig. 5.4

[4]

(ii) Draw on Fig. 5.4 to show how a potentiometer can be used as the volume control. Label the output of the volume control. **[3]**

(c) The input impedance of each block in Fig. 5.3 should be at least ten times the output impedance of the block to its left.
Explain why this is necessary.

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6 This question is about microcontroller systems.

Explain the function of the following parts of a microcontroller system:

(a) input port

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(b) register

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(c) host computer

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(d) analogue-to-digital converter

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.... **[2]**

(e) program.

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.... **[3]**

Quality of written communication [3]

END OF QUESTION PAPER

ADDITIONAL ANSWER SPACE

If additional space is required, you should use the following lined page(s). The question number(s) must be clearly shown in the margin(s).