OCR
Oxford Cambridge and RSA

GCE

Electronics

Unit **F612:** Signal Processors

Advanced Subsidiary GCE

Mark Scheme for June 2017

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This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by examiners. It does not indicate the details of the discussions which took place at an examiners' meeting before marking commenced.

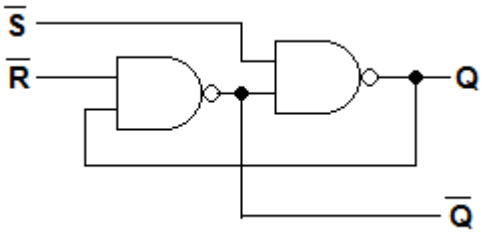
All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

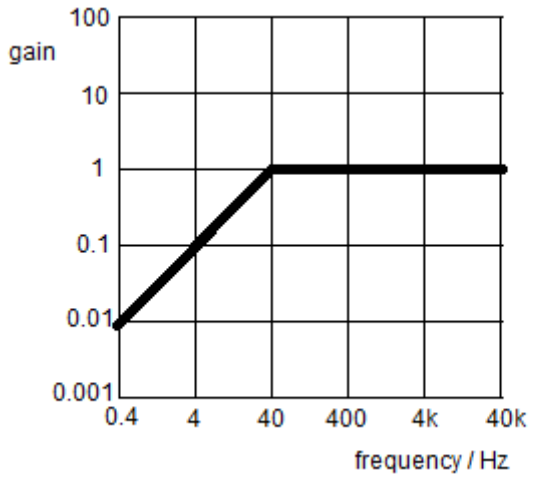
Mark schemes should be read in conjunction with the published question papers and the report on the examination.

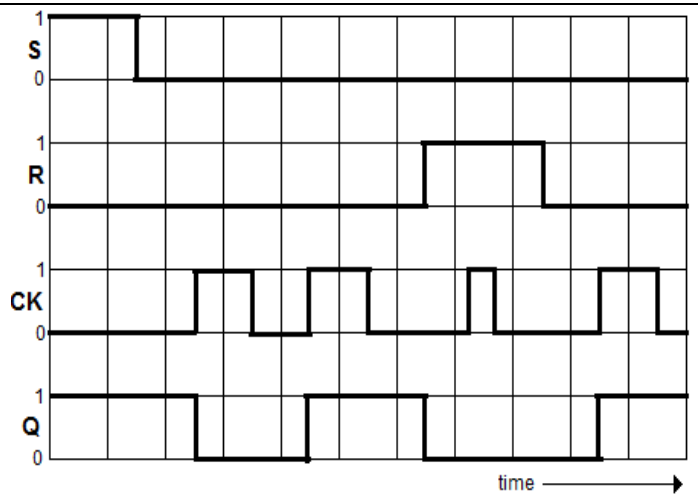
OCR will not enter into any discussion or correspondence in connection with this mark scheme.

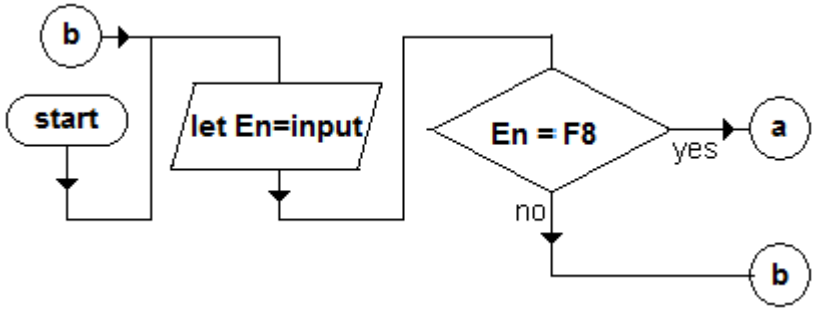
Annotations

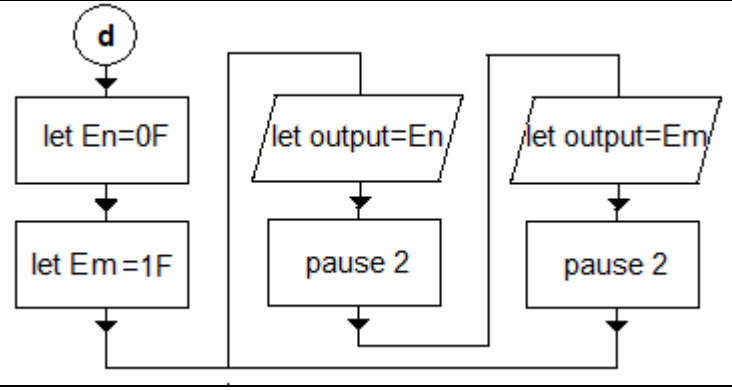
1	BOD	31	BOD	Benefit of doubt
2		21	Cross	Cross
3	ECF	241	ECF	Error carried forward
4	NBOD	191	NBOD	Benefit of doubt not given
5		1841	Not Relevant	Expandable vertical wavy line
6	REP	271	REP	Repeat
7	TV	201	TV	Too vague
8		11	Tick	Tick
9	0	1741	ZERO	Zero (big)
10				
11				
12				
13				
14				

<table>
<tr><th colspan="3">Question</th><th>Answer</th><th>Marks</th><th>Guidance</th></tr>
<tr><td>1</td><td>a</td><td>i</td><td>
<table>
<tr><th>$\overline{S}$</th><th>$\overline{R}$</th><th>Q</th><th>$\overline{Q}$</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>no change</td><td>no change</td></tr>
</table>
</td><td>3</td><td>Q and $\overline{Q}$ opposite states in first two rows [1]
correct inputs for first two rows [1]
correct inputs for third row [1]</td></tr>
<tr><td></td><td></td><td>ii</td><td>
<table>
<tr><th>B</th><th>A</th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td><td>2</td><td>all four input combinations (any order) [1]
correct output column [1]</td></tr>
<tr><td></td><td></td><td>iii</td><td> 
</td><td>3</td><td>correct NAND gate symbols [1]
output of each gate provides one input of the other [1]
correct labelling of inputs and outputs [1]
accept NAND gate as inverter from Q</td></tr>
<tr><td></td><td>b</td><td></td><td>D same as Q when clock/enable is high for a latch;
Q becomes same as D when clock rises (from 0 to 1) for a flip-flop;</td><td>1
1</td><td></td></tr>
</table>

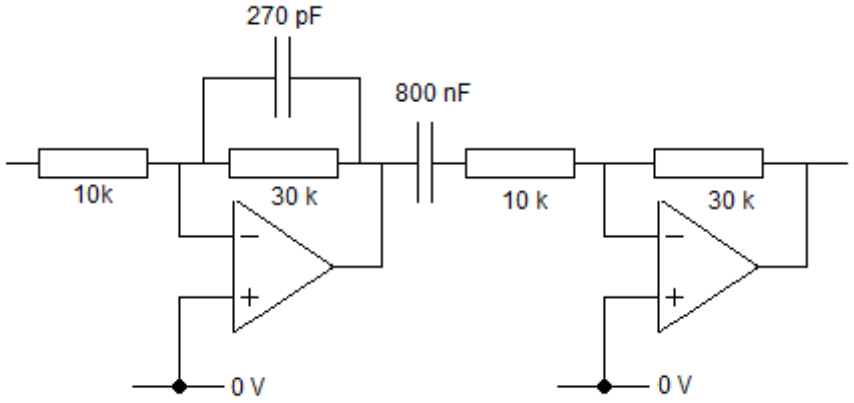
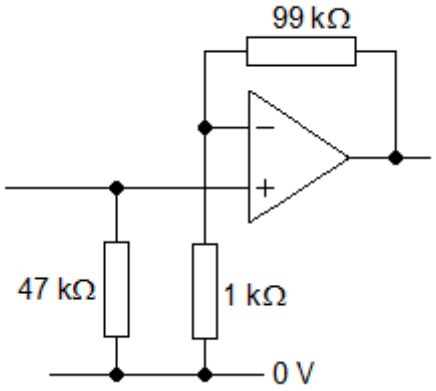
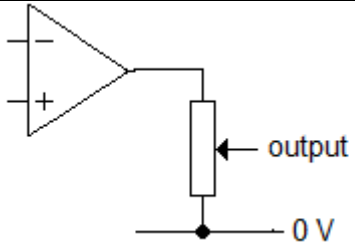
Question			Answer	Marks	Guidance
2	a	i	use of $f_0 = \frac{1}{2\pi RC}$; f_0 = 41 Hz;	1 1	correct substitution of values with powers of ten no mark for numerical answer alone.
		ii		1 1	gain of 1 above 40 Hz gain drops at 45 degrees below break frequency
		iii	• impedance of capacitor falls with increasing frequency / impedance of capacitor is $1/2\pi fC$ • resistor-capacitor network acts as a voltage divider; • above 40 Hz, resistor (constant) is dominant • below 40 Hz, capacitor is dominant	3	any **three** points: wtte wtte
	b	i	1(.00)	1	
		ii	op-amp has very large (open-loop) gain; negative feedback keeps **T** and **U** at same voltage;	1 1	
	c		power / current amplifier; to drive speaker; tone control to remove bass/low frequencies;	1 1 1	

Question			Answer	Marks	Guidance
3	a	i		1 1 1	Q high when S is high Q low when R is high Q changes on rising edges of CK when SR = 00
		ii	**D** is opposite of **Q / D**= Not **Q** **D** transfers to **Q** only on rising-edge of **CK**; **Q** changes state on each clock pulse	1 1 1	
	b	i	square wave / train of rising edges / alternates between 1 and 0; with a frequency of 2 Hz / period of 0.5s	1 1	no marks for naming the device e.g. oscillator, astable
		ii	(binary to seven segment) decoder	1	
		iii	sequence starts with 1; because **P** going high sets **A** and resets **B** and **C**; then 2,3,4 and 5; incrementing every 0.5s sequence 1 – 5 repeats continuously	1 1 1 1 1	

<table>
<tr><th colspan="3">Question</th><th>Answer</th><th>Marks</th><th>Guidance</th></tr>
<tr><td>4</td><td>a</td><td></td><td>
<table>
<tr><th>switches pressed</th><th>binary</th><th>hexadecimal</th></tr>
<tr><td>none</td><td>11101000</td><td>E8</td></tr>
<tr><td>both</td><td>11110000</td><td>F0</td></tr>
</table>
</td><td>1
1</td><td></td></tr>
<tr><td></td><td>b</td><td></td><td> 
</td><td>1
1
1
1</td><td>start box
input box
decision box
a and b consistent with yes and no

n can be any integer</td></tr>
<tr><td></td><td>c</td><td></td><td>waits for 8 s;
loads (0000)1010 / equivalent of decimal ten into S1
repeats last two steps if switch B is being pressed;
LEDs display counts down in binary from ten;
changing at intervals of 50 ms;
if B is pressed, program stops (and display freezes);
otherwise passes control to d when LEDs display zero;</td><td>1
1
1
1
1
1
1</td><td></td></tr>
<tr><td></td><td>d</td><td></td><td> 
</td><td>
1
1
1
1
1</td><td>m and n are any two different integers

continuous loop alternating states of output port
with a period of 4 ms
keeping LEDs on
turning MOSFET on and off
correct syntax, symbols and arrows</td></tr>
</table>

Question			Answer	Marks	Guidance
5	a			1 1 1 1 1 1 1 1	both 0 V labels / earth symbols all resistors between 100 Ω and 10 MΩ correct circuit for treble cut filter with $RC = 8.0\times10^{-6}$ s correct circuit for bass cut filter connected in series with $RC = 8.0\times10^{-3}$ s use of $f_0 = \frac{1}{2\pi RC}$ to justify values overall gain 9 at 2 kHz
	b	i		1 1 1 1	correct circuit input impedance of 47 kΩ gain of +100 use of $G = 1 + \frac{R_f}{R_{in}}$ to justify values
		ii		1 1 1	correct symbol connected between output of op-amp and 0 V wiper labelled as output

		c	output and next input impedances form a potential divider some signal lost across output impedance most signal from one block gets into the next if the ratio is at least 10:1	1 1 1	wtte

Question			Answer	Marks	Guidance
6	a		set of terminals/pins; which can be used to input binary **words** to the system;	1 1	
	b		holds a binary **word**; which can be: • processed during program • placed on output port / read from input port • for an address • for a program instruction	1 2	 any two from
	c		translates / compiles program; from flowchart / verbal / high level language into hexadecimal / binary; and downloads into microcontroller;	1 1 1 1	
	d		creates a binary word / number / code representing the voltage of a signal;	1 1	not converts analogue to digital
	e		(set of) instructions in memory of microcontroller; which fix its behaviour;	1 1 1	 wtte

APPENDIX 1

Quality of Written Communication

3	The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.
2	The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.
1	The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.
0	The language has no rewardable features.

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