



GCE

Electronics

Unit **F614**: Electronic Control Systems

Advanced GCE

Mark Scheme for June 2018

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This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by examiners. It does not indicate the details of the discussions which took place at an examiners' meeting before marking commenced.

All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

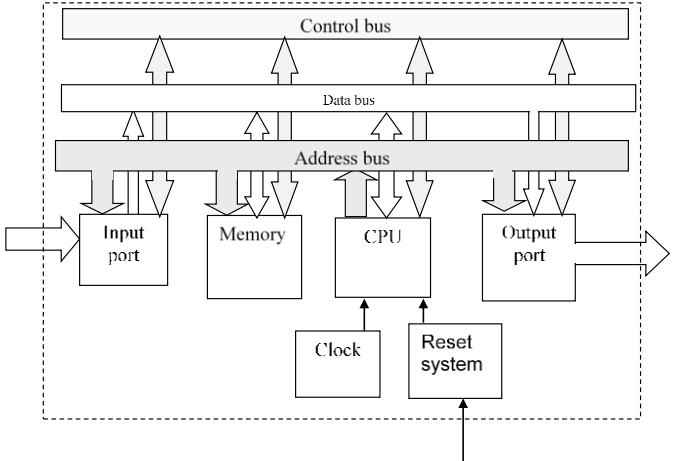
Mark schemes should be read in conjunction with the published question papers and the report on the examination.

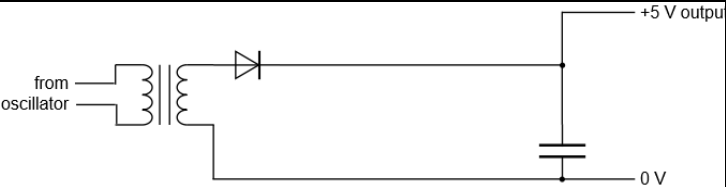
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Annotations

1		31	BOD	Benefit of doubt
2		21	Cross	Cross
3		241	ECF	Error carried forward
4		191	NBOD	Benefit of doubt not given
5		1841	Not Relevant	Expandable vertical wavy line
6		271	REP	Repeat
7		201	TV	Too vague
8		11	Tick	Tick
9		1741	ZERO	Zero (big)
10				
11				
12				
13				
14				

Question	Grade	Expected answer	Mark	Additional guidance
1a	E	capacitor	1	
	E	labelled V_{out} connection to D	1	
1b	C	calculate current $I = 3.5/220 \times 10^3 =$	1	
	B	1.59×10^{-5}	1	
	D	calculate voltage across R $V = 9 - 3.5 = 5.5$ V	1	
		calculate $R = 5.5/1.59 \times 10^{-5} = 3.46 \times 10^5 = 350$ k Ω		
1ci	E	Value between 2.2 V and 2.3 V	1	
1cii	E	current from graph 50 mA	1	
	C	voltage across 75 Ω resistor 3.75 V	1	
	A	$V_D = 9 - 3.75 = 5.25$ V	1	
1ciii	E	correct units conversion	1	
	C	find ΔV	1	
	B	divide current by voltage to calculate $g_m = 0.04$ S (ecf)	1	
1civ	D	$-g_m$ from 1ciii	1	
	D	x 75 Ω	1	

Question	Grade	Expected answer	Mark	Additional guidance
1di	E A D D A B	V_G : Sine wave amplitude 0.5 V Centred around 3.5 V Period 0.5 ms V_D : Wave the same shape as V_G amplitude 1.5 V Centred around 5.25 V (or 5 V) In anti-phase with V_G	1 1 1 1 1 1	Sine wave between 3 V and 5 V Wave shape of V_G between 6.75 V (6.5 V) and 3.75 V (3.5 V)
2a	E C C D D E E	CPU correct Data bus correct Address bus correct Input port Output port Memory Clock	1 1 1 1 1 1 1	(If address and data bus wrong way around 1 mark) 

Question	Grade	Expected answer	Mark	Additional guidance
2b	E	Group of wires	1	Any valid comment about address or location Not to CPU
	D	Carrying <u>location/address</u> of data to be stored/fetched	1	
	D	<u>from</u> CPU	1	
2c	E	Memory/register	1	
	D	in CPU	1	
	D	holding address of <u>next</u> instruction	1	
2d	D	Fetches instruction	1	Clarity needed in explanation
	C	from memory (pointed at by PC)	1	
	C	Increment PC	1	
	E	Execute instruction	1	
	B	Sequence correct (Fetch, increment, execute)	1	
3a	E	Path showing flow of information from output back to oscillator (wtte)	1	
3b	B	The output of an open loop system does not change when the conditions change/closed loop changes when condition change	1	
	C	Closed loop systems automatically adjust to keep the output at the desired level (owtte)	1	
3c	E	correct rectifier	1	
	E	correct polarity of output	1	
	E	capacitor for smoothing on dc output	1	

Question	Grade	Expected answer	Mark	Additional guidance
3d	E	<u>LED</u>	1	accept photo-diode
	E	<u>photo-transistor</u>	1	
	E	LED give out light when current/voltage present	1	
	D	photo-x switches on/conducts when receives light	1	
3ei	E	Correct zener symbol	1	
	C	Reverse biased	1	
	E	In series with resistor from smoothed supply	1	
	C	Producing 2.7 V at non-inverting input of comparator	1	
3eii	A*	when the smoother voltage was <5 V	1	Potential divider produces 2.7 V at correct output V If 5 V Zener used output would not switch until much higher voltage
	A*	an accurate reference would not be produced	1	
4a	E	rel: IN Sn, I	1	n=0-7 Accept addition of extra line MOVI Sr,20 AND Sn, Sr Must jump to correct line
	E	AND Sn, S1	1	
	D	JNZ rel	1	
	E	RET	1	
4b	EC	on: MOVI Sm, 1F	2	1 mark for MOVI, 1 mark for value accept 3F/7F/FF m=0-7
	E	OUT Q, Sm	1	
	E	RET	1	
4c	A	wait125ms: MOVI Sq, 7D	1	q=0-7 call and label Must jump back correctly to second line and include RET
	E	label: RCALL wait1ms	1	
	E	DEC Sq	1	
	C	JNZ label RET	1	

Question	Grade	Expected answer	Mark	Additional guidance
4d	C	Turn on first LED	1	run: MOVI S0, 01
	A	Turn on second LED	1	nxt: OUT Q, S0
	A*	Correct sequence	1	RCALL wait125ms
	C	Delay of 125 ms between elements of sequence	1	SHL S0
	E	RET at end of subroutine	1	MOVI S7, 20 SUB S7, S0 JNZ nxt RET
5a	E	Resistance falls as temperature rises	1	
5b	E	Total $R = 23 \times 10^3 + 28 \times 10^3 = 51 \times 10^3$	1	or any potential divider formula with correct answer [3]
	E	$I = 15 / 51 \times 10^3 = 2.94 \times 10^{-4} \text{A}$	1	
	E	$V = 2.94 \times 10^{-4} \times 28 \times 10^3 = 8.23 \text{V}$	1	
5c	D D C E	Any 4 of following: non-inverting input > inverting input OR $V_R > V_T$ Y output (saturated) high (OR +13V) VGS > threshold MOSFET conducting OR MOSFET has low resistance OR V_D is low current in heater OR voltage across heater	4	

Question	Grade	Expected answer	Mark	Additional guidance
5di	A B A B	Any 4 of following: <ul style="list-style-type: none"> • Turns off when too hot/turns on when too cold • Explanation of why heater turn off reference to voltages in circuit • It takes time for oven to warm/cool • It takes time for the thermistor to respond • Oven keeps cooling/warming for some time even when heater off/on • Full power or off • Constantly turning on and off • Temperature overshoots/undershoots as consequence of above 	1 1 1 1	
5(dii)	A* A* A* A* A* A*	T hunts around 8 V Y saturates +/-13 V (by eye between 10 V and 15 V lines) in time with X but antiphase D saturates 0 V and +15 V D square wave in antiphase with Y	1 1 1 1 1 1	any amplitude and period (not nec. constant)
6(a)	E	$2^4 = 16$	1	
6(b)	E	$11_2 = 3$	1	

Question	Grade	Expected answer	Mark	Additional guidance
6(c)	CE	$A_3 - A_0 = 0V, 0V, 5V, 0V$	2	Accept 0010 for [1] Accept any combination of 5V and 0V for [1]
	C	$\overline{CE} = 0V$	1	
	D	$\overline{Read} = 0V$	1	
	D	$\overline{Write} = 5V$	1	
6(d)	B	(ce, write and read all high) $A_3 - A_0 = 0111$	1	order of address and data unimportant Write pulled low Enabled pulsed low
	B	$D_1 - D_0 = 11$	1	
	A	enable pulled low	1	
	A	write pulsed low	1	
	A*	order correct (enable pulled high)	1	
6(e)	C	2 memory modules connected to power supplies	1	[1] A4 and CE gated to modules [2] A4 and CE gated to so that A4 selects module according to A4 when CE active
	B	data lines connected together	1	
	A	four address lines connected together	1	
	A*	fifth used to direct CE	1	
	A*	CE directed correctly	1	
	B	read and write connected together	1	

Quality of Written Communication

- 3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.
- 2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.
- 1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.
- 0 The language has no rewardable features.

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