OCR
Oxford Cambridge and RSA

GCE

Electronics

Unit **F612:** Signal Processors

Advanced Subsidiary GCE

Mark Scheme for June 2018

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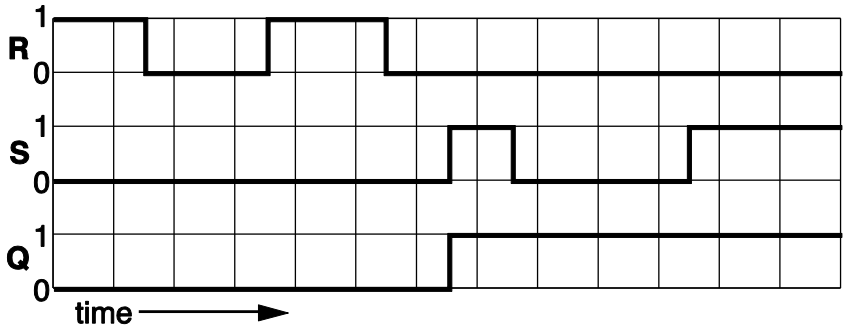
This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by examiners. It does not indicate the details of the discussions which took place at an examiners' meeting before marking commenced.

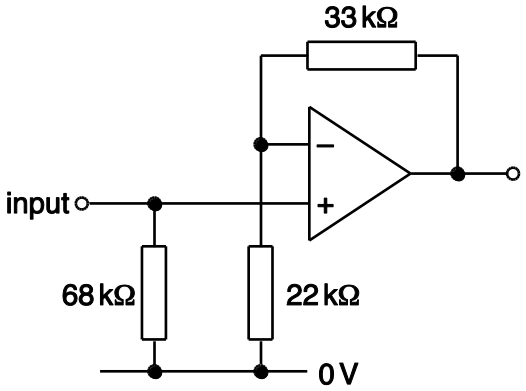
All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

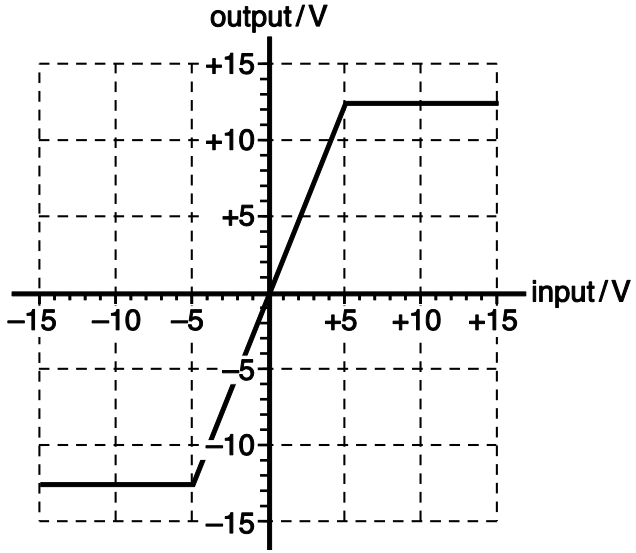
Mark schemes should be read in conjunction with the published question papers and the report on the examination.

Annotations

1		31	BOD	Benefit of doubt
2		21	Cross	Cross
3		241	ECF	Error carried forward
4		191	NBOD	Benefit of doubt not given
5		1841	Not Relevant	Expandable vertical wavy line
6		271	REP	Repeat
7		201	TV	Too vague
8		11	Tick	Tick
9		1741	ZERO	Zero (big)
10				

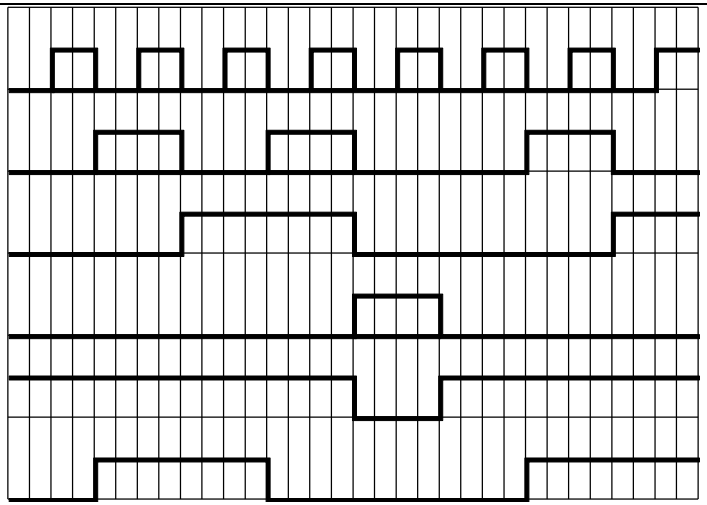
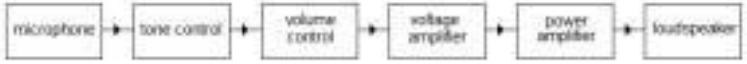
Question			Answer	Mark	Guidance
1	(a)		<table><tr><th>S</th><th>Q</th><th>P</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	2	all four input states (any order) for [1] THEN correct Q for [1]
1	(b)		Max 2 from: R goes high so Q goes low, both inputs S and Q are low making P high Led requires a PD/voltage across it	2	No ecf from incorrect truth table
1	(c)		LED (stays) off, P stays high because Q and S are low; Q is low because one input P is high.	1 1 1	Allow correct argument with LED stays on LED stays on P stays low because Q is high Q is high because P and R are low
1	(d)			2	Q is low until S goes high Q changes state on first rising edge of S (by eye) 1 mark for Q starting low, 1 mark for transition to high in correct place.

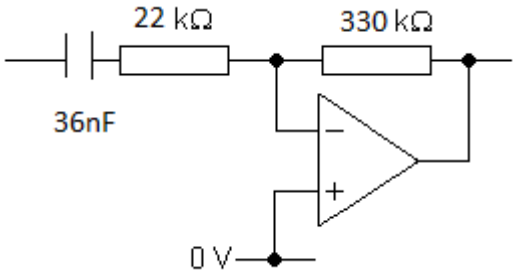
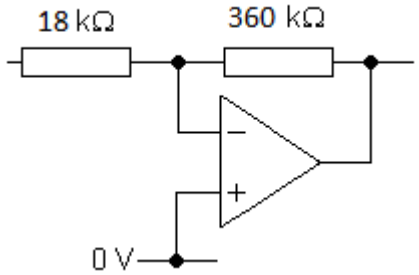
Question			Answer	Mark	Guidance
2	(a)		As a clock signal goes from 0 to 1 The input is transferred to the output	1 1	Rising edge Triggering of flip-flop
2	(b)	i	When clock goes low, X goes high, Therefore input is transferred to P (P goes high) Output stays low	1 1 1	
2	(b)	ii	Signal at P stays high Output goes high as P is transferred to Q.	1 1	
3	(a)	i		1	**not** next to + input **look for** the word INPUT near the circle **look for** the word OUTPUT
3	(a)	ii	68 kΩ	1	
3	(b)	i	1 + 33k/22k; 2.5;	1 1	quote and use correct formula with incorrect resistors from circuit (1) evaluation (1) (no ecf on incorrect formula or values)
3	(b)	ii	inverting input = 2.0 V; output = 5 V;	1 1	ecf gain of (b)(i) to output

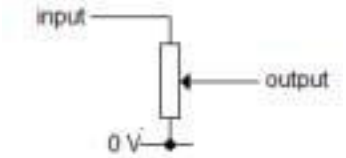
Question			Answer	Mark	Guidance
3	(b)	iii		3	straight line through the origin (1) correct gradient of +2.5 (1) **accept** gradient of gain of (b)(i) saturating at +13 V and - 13 V (1)
3	(c)		EITHER Difference in voltage between inputs; is amplified by a large amount. OR when V_+ less than V_- output is negative; when V_+ more than V_- output is positive; OR $V_{out} = A(V_+ - V_-)$ where A is large value; V_+ is non-inverting (+) input voltage, V_- is inverting (-) input voltage, THEN output saturates at ± 13 V;	2 1	**not** just differential amplifier **accept** A at least 1000

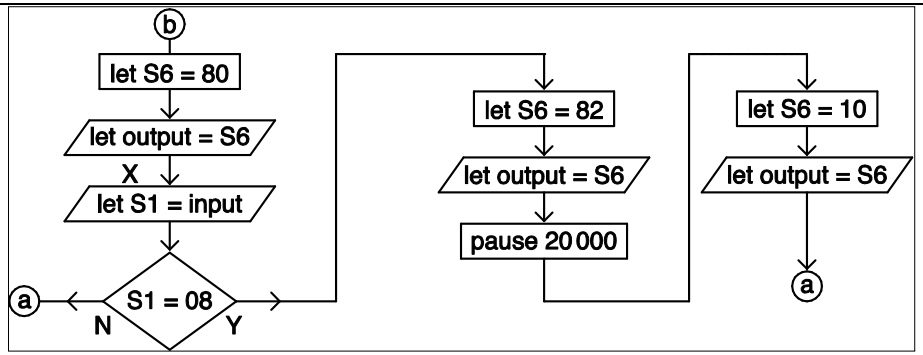
<table>
<tr><th colspan="3">Question</th><th>Answer</th><th>Mark</th><th>Guidance</th></tr>
<tr><td>4</td><td>(a)</td><td>i</td><td>$\overline{Q}$ to D on each flip-flop (no other connection to D)
$\overline{Q}$ to clock of next flip-flop(no other connection to CK)
clock input (ck) to clock of first flip-flop through NOT gate
counter outputs from Q of flip-flops
outputs labelled A, B and C from left to right</td><td>1
1

1
1
1</td><td></td></tr>
<tr><td>4</td><td>(a)</td><td>ii</td><td>Connections from A and C
to AND gate whose output goes to R on all flip-flops (no other connections to R)</td><td>1
1</td><td>ecf from (i)
ACCEPT R of first-flip-flop at 0 V all the time and AND gate to other two</td></tr>
<tr><td>4</td><td>(b)</td><td>i</td><td>Column X correct
Column Y correct
<table><tr><th>C</th><th>B</th><th>A</th><th>X</th><th>Y</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table></td><td>1
1</td><td></td></tr>
</table>

Question			Answer	Mark	Guidance
4	(b)	ii	 A correct all the way along B changes on first two falling edges of A C rises on first falling edge of B B and C go/stay low on fifth falling edge of CK X inverse of C Y high whenever A and B are not the same	1 1 1 1 1 1	
5	(a)		microphone first, loudspeaker last voltage amplifier somewhere before power amplifier tone control somewhere before power amplifier 	1 1 1	

Question			Answer	Mark	Guidance
5	(b)		correct circuit input through 22 kΩ resistor 330 kΩ feedback resistor 36 nF capacitor (accept 33 nF) use of break frequency formula to find *C* use of inverting amplifier gain formula to find R_f 	1 1 1 1 1 1	accept missing 0 V label ecf: 15 × incorrect input resistor for [1] allow ecf in calculating *C* for incorrect value of input resistor
5	(c)		inverting amplifier circuit resistors to give gain of 20 (either type of amp) use of gain formula for type of amplifier attempted 	1 1 1	0 V label must be present ignore range of resistor values

Question			Answer	Mark	Guidance
5	(d)		correct symbol one track end to 0 V other track end to input, wiper to output 	1 1 1	**ignore** any resistor or capacitors in series with input or output
6	(a)		<table><tr><td>0000 1000</td><td></td></tr><tr><td></td><td>48</td></tr><tr><td>0000 0000</td><td>00</td></tr></table>	3	each correct row for [1] **don't accept** missing leading 0s, penalise once
6	(b)	i	[S0 is 40 or 48 when train is moving] > 8 [S0 is 00 or 08 when train is stationary] ≤ 8	1 1	either argument,moving or stationary with reference to inequality. [1] for each value
6	(b)	ii	S6 loaded with 0001 0000; L off, DO low/0, DC high/1	1 1 1	

Question			Answer	Mark	Guidance
6	(c)			6	Load any register with 80 and output [1] Read input of 08 only [1] From **No:** return to a, b or loop to X From **yes:** make output port 82 (using any register) [1] pause 20 000 [1] output 10 [1] and return to a [1] **penalise** mistake in common code only once **penalise** incorrect syntax or box shape or lack of arrows only once **ignore** $ in front of hexadecimal words
7	(a)		when Q is low AND gate forces P low (as 0.X = 0) pulse at S copies 1 at D to Q so P = 1.X = X	1 1 1	AND gate blocks pulses when Q = 0 for [1] flip-flop copies 1 at D to Q when pulse at S for [1] AND gate transmits pulses when Q = 1 for [1]
7	(b)		any of the following for [1] each • pulses counted by binary counter • starting from 0000 • counter reset when Q = 0 • C / R goes high on fourth pulse • resetting flip-flop • forcing P to stay low again/stopping pulses getting through AND gate	4	

Question			Answer	Mark	Guidance
8	(a)		where bytes / words; enter **and** leave the microcontroller / copied to and from registers;	2	**look for** idea of sets of bits in parallel, not serial accept download a program for [1]
8	(b)		outputs/stores/creates a byte/word/binary code; which represents a voltage;	2	**not** just digital signal, high or low, 1 or 0, binary not analogue signal / wave / variable signal

8	(c)		any two of the following reason-explanation pairs, (1) + (1) each:
			• smaller circuit
			  • because only one chip
			• can be easily updated/changed
			  • because program easily changed
			• cheaper circuit
			  • because of economies of scale / mass production
			• easier to design
			  • because program can be simulated
			• different circuits from the same hardware
			  • because program can be loaded
				4	look for two reason-explanation pairs for full marks
					
					ignore reasons to do with supply rails

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