



GCE

Electronics

Unit **F614**: Electronic Control Systems

Advanced GCE

Mark Scheme for June 2014

OCR (Oxford Cambridge and RSA) is a leading UK awarding body, providing a wide range of qualifications to meet the needs of candidates of all ages and abilities. OCR qualifications include AS/A Levels, Diplomas, GCSEs, Cambridge Nationals, Cambridge Technicals, Functional Skills, Key Skills, Entry Level qualifications, NVQs and vocational qualifications in areas such as IT, business, languages, teaching/training, administration and secretarial skills.

It is also responsible for developing new specifications to meet national requirements and the needs of students and teachers. OCR is a not-for-profit organisation; any surplus made is invested back into the establishment to help towards the development of qualifications and support, which keep pace with the changing needs of today's society.

This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by examiners. It does not indicate the details of the discussions which took place at an examiners' meeting before marking commenced.

All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

Mark schemes should be read in conjunction with the published question papers and the report on the examination.

OCR will not enter into any discussion or correspondence in connection with this mark scheme.

© OCR 2014

Quality of Written Communication

- 3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.
- 2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.
- 1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.
- 0 The language has no rewardable features.

question	grade	expected answer	mark	additional guidance
1a	E	2.9 V	1	Allow 2.8 V – 2.9 V
1bi	D	G from switch is -5 V S is 0V so $V_{GS} = -5 V$	1	Resistance of MOSFET very high
	C	$V_{GS} < \text{threshold}$	1	
	C	so MOSFET not conducting	1	
1bii	E	line at 0 from $t=0$ to $t=4$	1	
	D	oscillation from 4 to end around 0V	1	
	D	same amplitude, shape and phase as input	1	

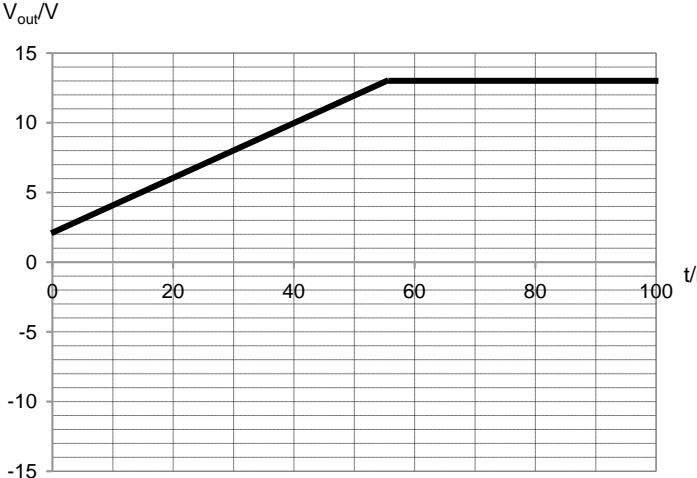
question	grade	expected answer	mark	additional guidance
2a	E	six D-type flip-flops	1	
	E	5 x Q to next D	1	
	E	clocks connected together and labelled	1	
	E	serial in correctly labelled at first D	1	
	E	outputs correctly labelled at all Qs	1	
2bi	C	first two clock periods correct	1	correct shape but changing on falling edge [2]
	D	periods 3 & 4 correct	1	
	A	periods 5, 6 correct	1	
		<p>The diagram shows two waveforms over time (t). The top waveform is labeled 'clock' and is a square wave with a period of 1 unit, alternating between 1 and 0. The bottom waveform is labeled 'Z' and is a square wave that is high (1) for the first two clock periods, low (0) for the next four clock periods, and high (1) for the last two clock periods. Vertical dashed lines indicate the falling edges of the clock signal, which correspond to the state changes in the Z signal.</p>		
2bii	A	110001 no ecf	1	beware of reversing order of bits
2biii	C	49 (ecf from bii)	1	

question	grade	expected answer	mark	additional guidance
3a	A E B C E	go: MOVI Sn, 04 IN Sm, I AND Sn, Sm JZ go RET	1 1 1 1 1	n≠m n&m≤7 OR AND Sm, Sn Lose 1 mark if SUB Sm, Sn JNZ go (does not work if X pressed or other I float high)
3b	C B B	44 4C 55 5D 77 first one correct next two correct last two correct	1 1 1	
3c	D C A D B E E	Max 7 of: Initialise pointer to start of look-up table output number from table move pointer to next item in table check to see if at end of table if so reset to start of table Mask for X check to see if switch is pressed if not go back and output next number from table if pressed return to main program	7	Make dice show 1 Allow loop 6 times owtte

question	grade	expected answer	mark	additional guidance
3d	D	make Q7 high	1	$0 < j \leq 7, 0 < k \leq 7, j \neq k$
	B	without changing Q0-Q6	1	beep: <code>MOVI Sk, 80</code>
	C	initialise counter with C8 (hex for 200)	1	
	C	time delay	1	<code>EOR S0, Sk</code>
	A	make Q7 low without changing Q0-Q6	1	<code>OUT Q, S0</code>
	E	return	1	<code>MOVI Sj, C8</code> <code>lbl: RCALL wait1ms</code> <code>DEC Sj</code> <code>JNZ lbl</code> <code>EOR S0, Sk</code> <code>OUT Q, S0</code> <code>RET</code>

question	grade	expected answer	mark	additional guidance
4a	E E	diodes used to produce rectifier with correct polarity	1 1	<p>The first diagram shows a half-wave rectifier circuit with an AC supply connected to a single diode. The output is taken across a capacitor connected to the diode's cathode and the common ground (0V). The output is labeled '+V unregulated dc'.</p> <p>The second diagram, labeled 'OR', shows a full-wave bridge rectifier circuit with an AC supply connected to a bridge of four diodes. The output is taken across a capacitor connected between the positive and negative output terminals of the bridge and the common ground (0V). The output is labeled '+V unregulated dc'.</p> <p>capacitor used in parallel with output or in 4(c)</p>
4b	CD	Max 2 of: unregulated has (a large) ripple (wtte) unregulated output voltage depends on ac input (wtte) regulated output has no/very little ripple (wtte) regulated output fixed/not dependent on input (wtte) regulator keeps the voltage at a constant voltage (wtte)	2	
4c	C C A A	correct reference with zener and resistor connected to op-amp input MOSFET used correctly at output negative feedback from regulated output	1 1 1 1	

question	grade	expected answer	mark	additional guidance
5a	E	total R = 22k + 47k	1	
	E	$I = 6/69000 = 0.087 \text{ mA}$	1	
	E	$0.000087 \times 47000 = 4.09 \text{ V}$	1	
5b	C	motor off until G = 1.8 V	1	
	E	motor speeds up as G increases (from 1.8 V)	1	
	D	as current increases or any reasonable point about what happens above 1.8 V	1	
5c	C	Max 2: speed depends on load (wtte)	1	
	B	no feedback to monitor speed speed depends on supply voltage speed depends on MOSFET temp	1	
5di	CCD DEE	1 mark for each correct label	6	<pre> graph LR reference[reference] --> diff_amp[difference amplifier] diff_amp --> ramp_gen[ramp generator] ramp_gen --> power_amp[power amplifier] power_amp --> motor[motor] motor -.-> speed_sensor[speed sensor] speed_sensor --> diff_amp </pre>
5dii	ABC	Max 3 of: output of difference amp non zero output of ramp generator goes up supply to motor increases	3	

question	grade	expected answer	mark	additional guidance
5e	D C B A	line of constant positive slope from 2 V attempt to use correct ramp generator formula gradient 4 V in 20 ms saturates at +13 V (ecf)	1 1 1 1	 <p>The graph shows the output voltage V_{out} in Volts on the y-axis versus time t in milliseconds on the x-axis. The y-axis ranges from -15 to 15 with major grid lines every 5 units and minor grid lines every 1 unit. The x-axis ranges from 0 to 100 with major grid lines every 20 units and minor grid lines every 2 units. The plotted line starts at (0, 2), increases linearly to (60, 13), and then remains constant at 13 V until $t = 100$ ms.</p>

question	grade	expected answer	mark	additional guidance
6a	DDEE	Max 4 of: <ul style="list-style-type: none"> • subroutines can be re-used • subroutines can be tested separately • programs easier to read • programs easier to write due to structure • saves memory because subroutine only needs to be stored once 	4	1 mark for state, 1 mark for explain
6b	C	value retrieved from stack	1	
	C	and stored in program counter to instruction after RCALL	1	
	A	stack pointer changed by 1	1	
6c	A*	instructions unchanged	1	Allow 2D
	A*	program counter = 2E	1	
	A*	stack pointer changed by 1 (56 or 58)	1	
	A*	all but one data value unchanged	1	
	A*	one data value now 2C (address 56, 57 or 58)	1	

question	grade	expected answer	mark	additional guidance
7a	E E E	input connected to V_G output connected to V_D each input connected through a capacitor	1 1 1	<p>18 V</p> <p>200Ω</p> <p>input</p> <p>R</p> <p>V_D</p> <p>V_G</p> <p>470kΩ</p> <p>0V</p> <p>output</p>
7bi	A B A	from graph $g_m = 0.05 \text{ S}$ $R = 200 \Omega$ gain = $- 0.05 \times 200 = -10$ (ecf g_m)	1 1 1	transconductance calculated 200 Ω used gain -ve
7bii	A* A* A* A* A* A*	V across 200 Ω : $18 - 10 = 8 \text{ V}$ $I = 8 / 200 = 0.04 \text{ A}$ from graph $V_G = 2.3 \text{ V}$ I in 470 k Ω : $2.3/470000 = 4.89 \mu\text{A}$ V across R: $10 - 2.3 = 7.7 \text{ V}$ (ecf from 8bii) $R = 7.7 / 4.89 \times 10^{-6} = 1600 \text{ k}\Omega$	1 1 1 1 1 1	
7c	A* A*	MOSFETs have different characteristics Affects bias design not so sensitive to different MOSFETs	1 1	

question	grade	expected answer	mark	additional guidance												
8ai	E E E	<table border="1"> <thead> <tr> <th>Q</th> <th>U</th> <th>L</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>open</td> <td>closed</td> </tr> <tr> <td>1</td> <td>closed</td> <td>open</td> </tr> <tr> <td>High impedance</td> <td>open</td> <td>open</td> </tr> </tbody> </table>	Q	U	L	0	open	closed	1	closed	open	High impedance	open	open	1 1 1	1 mark for each correct row
Q	U	L														
0	open	closed														
1	closed	open														
High impedance	open	open														
8aii	D D D	<p>logic to turn off both analogue switches with E</p> <p>logic turns off both analogue switches when E high</p> <p>logic turns reproduces A at Q (for one or more states of E)</p>	1 1 1	<p>E.g.</p> <p>5 V</p> <p>A</p> <p>E</p> <p>0 V</p> <p>Q</p> <p>or any other working logic</p>												
8b	D E	to disconnect the output from the bus so that more than memory can be connected to the same bus	1 1													
8c	E E E D D B	<p>tristates between on each Q</p> <p>2Qs to each Data line</p> <p>2Ds to each data line</p> <p>Read operates tristates</p> <p>write operates clocks</p> <p>A0 routes read and write correctly</p>	1 1 1 1 1 1													

question	grade	expected answer	mark	additional guidance
8d	E	information lost when power is turned off	1	

OCR (Oxford Cambridge and RSA Examinations)
1 Hills Road
Cambridge
CB1 2EU

OCR Customer Contact Centre

Education and Learning

Telephone: 01223 553998

Facsimile: 01223 552627

Email: general.qualifications@ocr.org.uk

www.ocr.org.uk

For staff training purposes and as part of our quality assurance programme your call may be recorded or monitored

Oxford Cambridge and RSA Examinations
is a Company Limited by Guarantee
Registered in England
Registered Office; 1 Hills Road, Cambridge, CB1 2EU
Registered Company Number: 3484466
OCR is an exempt Charity

OCR (Oxford Cambridge and RSA Examinations)
Head office
Telephone: 01223 552552
Facsimile: 01223 552553

© OCR 2014

