

**GCE**

**Electronics**

Unit **F612**: Signal Processors

Advanced Subsidiary GCE

**Mark Scheme for June 2016**

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All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

Mark schemes should be read in conjunction with the published question papers and the report on the examination.

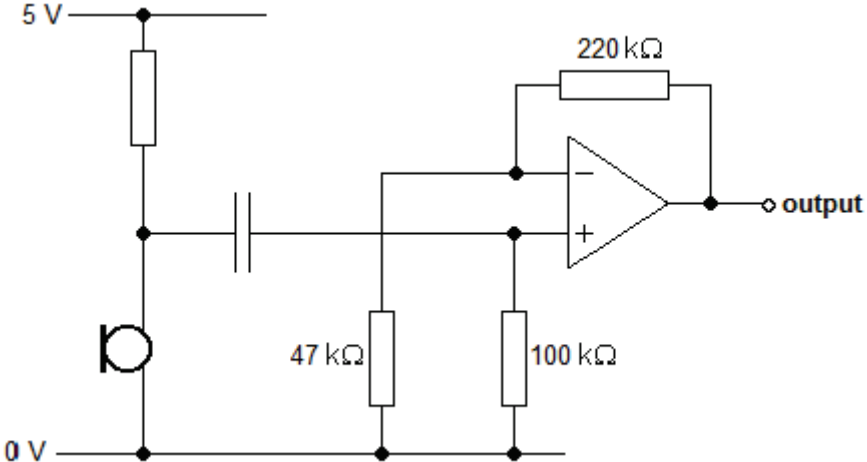
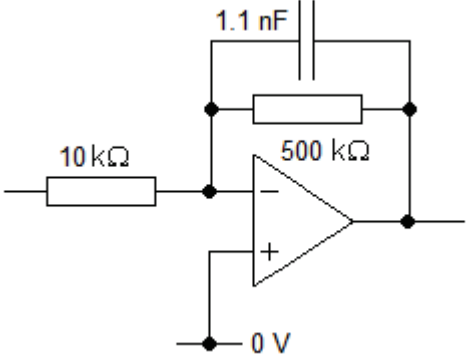
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## Annotations

	Annotation	Meaning of Annotation
1		Benefit of doubt
2		Cross
3		Error carried forward
4		Benefit of doubt not given
5		Expandable vertical wavy line
6		Repeat
7		Too vague
8		Tick
9		Zero (big)

Question			Answer	Marks	Guidance
1	a	i	still glows / stays on	1	
		ii	With M released; press (and then release) L.	1 1	
	b			2	correct feedback to make a bistable [1] correct connection of inputs [1]
Question			Answer	Marks	Guidance
2	a			1	completely correct for [1]
		b	when clock is low, output of bistable 2 is frozen / not transparent.; but bit at input can pass to P; as clock goes high, bit at P passes to output; when clock is high P is frozen / bistable 1 not transparent.	1 1 1 1	

Question	Answer	Marks	Guidance
3 a		2	correct symbols for microphone and capacitor [1] correct circuit [1]
b	gain = 5.7; amplitude = 284 mV; frequency = 450 Hz;	1 1 1	ecf: $G = -4.68$ gives (-) 234 mV for [1].
c	output saturates at 13 V; equivalent to an input of $13/5.7 = 2.3$ V	1 1	Evidence of appropriate calculation
d		6	correct circuit [1] resistors in range 1 kΩ to 1 MΩ [1] $R_F/R_{IN} = 50$ [1] justified by quoting and using $G = (-)\frac{R_F}{R_{IN}}$ [1] $R_F C = 530 \mu\text{s}$ [1]. justified by quoting and using $f_o = \frac{1}{2\pi RC}$ [1]

Question		Answer	Marks	Guidance																																								
4	a	$C = \frac{500 \times 10^{-3}}{0.5 \times 33 \times 10^3} = 30 \mu F$	2	correct use of $T = 0.5RC$ (evidence of rule) [1] correct answer [1]																																								
	b	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>P</th> <th>C</th> <th>B</th> <th>A</th> <th>X</th> <th>Y</th> <th>Z</th> <th>R</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>2</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>3</td> <td>0</td> <td>1</td> <td>1</td> <td style="background-color: #cccccc;"></td> <td style="background-color: #cccccc;"></td> <td style="background-color: #cccccc;"></td> <td>1</td> </tr> </tbody> </table>	P	C	B	A	X	Y	Z	R	0	0	0	0	1	1	1	0	1	0	0	1	0	1	1	0	2	0	1	0	0	0	1	0	3	0	1	1				1	3	B column correct for [1] A and C columns correct for [1] X, Y and Z columns correct for [1]  ignore content of grey squares
P	C	B	A	X	Y	Z	R																																					
0	0	0	0	1	1	1	0																																					
1	0	0	1	0	1	1	0																																					
2	0	1	0	0	0	1	0																																					
3	0	1	1				1																																					
	c	i	AND gate output to R; Inputs B and A;	1 1	ecf from (b).																																							
		ii	$X = \overline{C+B+A};$ $Y = \overline{C+B};$ $Z = \overline{C.(B.A)};$	1 1 1	ecf from (b).																																							

Question		Answer	Marks	Guidance		
5	a	variable gain; between 0 and 1; blocks low frequencies / dc;	1 1 1			
	b		3	correct circuit [1] correct value resistors [1]  quote and use $-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2}$ [1]		
	c	i			4	calculated break frequency of 2 kHz [1] gain of 1 below break frequency [1] gain drops at 45° above break frequency [1] logarithmic scale on horizontal axis [1]
		ii		removes <u>high</u> frequencies / <u>treble</u> ;  EITHER: reducing high frequency noise / hiss OR: to match characteristics of loudspeaker OR: to allow the sound to have the correct <u>frequency</u> balance	1 1	
	d	i		increase the current (delivered to loudspeaker); EITHER: loudspeaker has a low input impedance/ resistance OR: tone control outputs small current only.	1 1	not "increase power"
		ii		0 V; negative feedback; maintains same voltage at both inputs of op-amp; because of high (open-loop ) gain of the op-amp;	1 1 1 1	not "infinite gain"

Question		Answer	Marks	Guidance
6	a	<p>Any 3 of the following [1] each:</p> <ul style="list-style-type: none"> <li>input to X (from counter/DCBA) is a 4 bit / binary number/word</li> <li>output (gfedcba) produces codes for a decimal number</li> <li>LEDs / 7-seg display decimal number (0 – 9)</li> <li>X contains drivers for LEDs</li> <li>X contains logic gates to convert each input word to required output word;</li> </ul>	3	
	b	<p>The diagram shows four digital signals over time, marked by a grid. The vertical axis for each signal is labeled 0 and 1. The horizontal axis is labeled 'time' with an arrow pointing right. Signal P is a square wave that starts at 1, drops to 0 at the end of each of the first 7 pulses, and then stays at 0. Signal A starts at 1 and drops to 0 on the falling edge of P. Signal B starts at 0 and goes high (1) at the first falling edge of P, staying high until the 4th falling edge of P, then drops to 0. Signal C starts at 0 and has a single pulse (goes high to 1) at the end of the 7th pulse of P, then returns to 0.</p>	4	<p>A changes only on each falling edge of P [1]                      B changes on each falling edge of A [1]                      C goes high at end of 7th square [1]                      A, B and C low in 8th and 9th squares [1]</p> <p>Award marks, as appropriate, to answers which begin with A=0.</p>
	c	<p>pulse/rising edge at G copies 5 V at D to Q;                      pulses/falling edges at P recorded/counted by counter;                      (LED) display shows 1 then 2 then 3;                      then C goes high / after 4 pulses, flip-flop resets, so no more pulses at P;  <math>\bar{Q}</math> goes high and resets counter / display shows zero;</p>	<p>1                      1                      1                      1                      1</p>	Not binary equivalent



Question			Answer	Marks	Guidance
7	a	i		3	inputs identified [1] outputs identified [1] clocks joined in parallel and labelled [1]
	a	ii	any <b>three</b> of the following, [1] each: <ul style="list-style-type: none"> <li>• hold a word/code copied from input port;</li> <li>• hold a word from the ADC;</li> <li>• hold address of memory location;</li> <li>• hold a (program) instruction;</li> <li>• be used in calculations;</li> <li>• be used for comparisons.</li> </ul>	3	Not 'to output port', because given in question
	b		hardware is circuit components (inside microcontroller); software is program/instructions (loaded into memory);	1 1	Words to that effect “

Question			Answer	Marks	Guidance
8	a	i	<pre> graph TD     Start([start]) --&gt; Process[let S0 = 80]     Process --&gt; Output[/let output = S0/]     A((a)) --&gt; Arrow[ ]     style Arrow width:0px,height:0px     Arrow --- Process           </pre>	2	<p>correct byte in process box. First 'nibble' must be 8, second 'nibble' consistent with <math>O_1=0</math> [1]</p> <p>correct output box [1]</p> <p>Look for correct use of capitals and lower case</p>
		ii	D0 is 1101 0000; LED y is on / glows; left lamp cluster activated;	1 1 1	Not with x and/or z Not with right cluster
	b	i	Let $S_n = \text{input}$ ; $S_n = 08$ ;	1 1	n must be an integer, not 1, 2 or 3 not "8"
		ii	(places three in S4 to use as a counter); activates left cluster and LED y for 125 ms; turns off cluster and LED for 125 ms; reduces S4 by one then goes to c if S4 has reached zero; otherwise switch cluster and LED on and off again; so cluster and LED flash on and off three times	1 1 1 1 1	ecf (a)(ii)

Question	Answer	Marks	Guidance
<p>8    c</p>	<pre> graph TD     c((c)) --&gt; S5[Let S5 = input]     S5 --&gt; D{S5 = 40}     D -- yes --&gt; S1[let output=S1]     D -- yes --&gt; S0[let output=S0]     S1 --&gt; P1[pause 250]     S0 --&gt; P2[pause 250]     P1 --&gt; J(( ))     P2 --&gt; J     J --&gt; S5     D -- no --&gt; e((e))     </pre>	<p>4</p>	<p>uses Sn (n&gt;4) to test input port for 40 [1]          if 'yes', outputs S1 (12) followed by 250ms delay, then S0 (80) followed by 250ms delay, then returns to c [1]          if 'no' then returns to e [1]          correct shaped boxes and use of arrows [1]</p>

## APPENDIX 1

## Quality of Written Communication

3	The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.
2	The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.
1	The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.
0	The language has no rewardable features.

**OCR (Oxford Cambridge and RSA Examinations)**  
**1 Hills Road**  
**Cambridge**  
**CB1 2EU**

**OCR Customer Contact Centre**

**Education and Learning**

Telephone: 01223 553998

Facsimile: 01223 552627

Email: [general.qualifications@ocr.org.uk](mailto:general.qualifications@ocr.org.uk)

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**Head office**  
**Telephone: 01223 552552**  
**Facsimile: 01223 552553**

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