

# **SPECIMEN**

**Advanced GCE** 

**F615 QP** 

**Electronics** 

Unit F615: Communications Systems

**Specimen Paper** 

Candidates answer on the question paper. Additional Materials:

Scientific calculator

Time: 1 hour 40 mins

Candidate Name	
Contro	Condidate
Centre Number	Candidate Number

#### **INSTRUCTIONS TO CANDIDATES**

- Write your name, Centre number and Candidate number in the boxes above.
- Answer all the questions.
- Use blue or black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure you know what you have to do before starting your answer.
- Do not write in the bar code.
- Do **not** write outside the box bordering each page.
- WRITE YOUR ANSWER TO EACH QUESTION IN THE SPACE PROVIDED.

#### **INFORMATION FOR CANDIDATES**

- The number of marks is given in brackets [] at the end of each question or part question.
- You will be awarded marks for the quality of written communication where this is indicated in the question.
- You may use a scientific calculator.
- Unless otherwise indicated, you can assume that :
  - op-amps are run off supply rails at +15 V and -15 V
  - logic circuits are run off supply rails at +5 V and 0 V
- You are advised to show all the steps in any calculations.
- The total number of marks for this paper is 110.

FOR EXAMINERS' USE					
Qu.	Max.	Mark			
1	17				
2	14				
3	17				
4	17				
5	23				
6	9				
7	13				
TOTAL	110				

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[Turn Over

### **Data Sheet**

resistance  $R = \frac{V}{I}$ 

power P = VI

series resistors  $R = R_1 + R_2$ 

time constant  $\tau = \textit{RC}$ 

monostable pulse time T = 0.7RC

relaxation oscillator period T = RC

frequency  $f = \frac{1}{T}$ 

voltage gain  $G = \frac{V_{out}}{V_{in}}$ 

open-loop op-amp Vout = A(V+ - V-)

non-inverting amplifier gain  $G = 1 + \frac{R_f}{R_d}$ 

inverting amplifier gain  $G = -\frac{R_f}{R_{in}}$ 

summing amplifier  $-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \dots$ 

break frequency  $f_0 = \frac{1}{2\pi RC}$ 

Boolean Algebra 
$$A.\overline{A} = 0$$

$$A + \overline{A} = 1$$

$$A.(B+C) = A.B + A.C$$

$$\overline{A.B} = \overline{A} + \overline{B}$$

$$\overline{A+B}=\overline{A}.\overline{B}$$

$$A + A.B = A$$

$$A.B + \overline{A}.C = A.B + \overline{A}.C + B.C$$

amplifier gain  $G = -g_m R_d$ 

ramp generator 
$$\Delta \textit{V}_{\textit{out}} = -\textit{V}_{\textit{in}} \, \frac{\Delta \textit{t}}{\textit{RC}}$$

inductor reactance  $X_L = 2\pi f L$ 

capacitor reactance 
$$X_C = \frac{1}{2\pi fC}$$

resonant frequency  $f_0 = \frac{1}{2\pi\sqrt{LC}}$ 

#### Answer all questions.

Unless otherwise indicated, you can assume that:

- op-amps are run off supply rails at +15 V and -15 V
- logic circuits are run off supply rails at +5 V and 0 V
- Fig. 1.1 is an amplitude-frequency graph for a carrier signal which is amplitude modulated by a test signal.

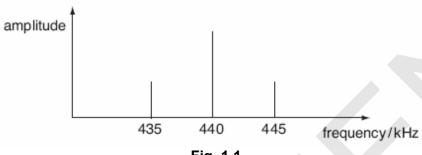


Fig. 1.1

State the frequency of the carrier signal.

frequency = ..... kHz [1] (ii) Explain how the graph shows that the frequency of the test signal is 5 kHz. ......[3]

(iii) Fig. 1.2 shows the amplitude modulated carrier seen on the screen of an oscilloscope.

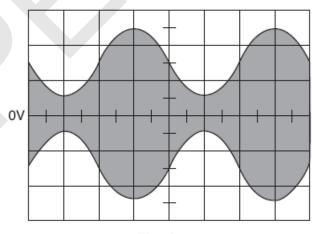
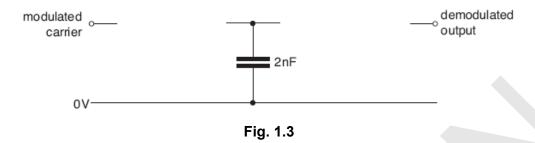


Fig. 1.2

Show that the timebase setting is 50  $\mu s$  per division.

- **(b)** The signal shown in Fig. 1.2 can be demodulated with a circuit containing these three components: **capacitor**, **diode**, **resistor**.
  - (i) Fig. 1.3 shows an incomplete demodulator circuit.

Complete the circuit by adding a diode and a resistor.



[2]

(ii) Explain why 30 kHz is a suitable choice of break frequency for the demodulator circuit.

......[2]

(iii) Calculate a suitable value for the resistor in the demodulator.

resistance = .....  $k\Omega$  [3]

(iv) The output of the demodulator circuit is connected to the input of the oscilloscope. The settings of the vertical amplifier and timebase are not changed. Sketch on Fig. 1.4 to show the waveform displayed on the oscilloscope screen.

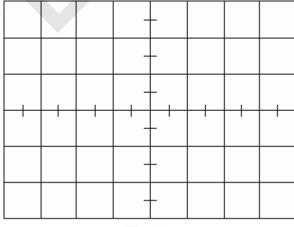


Fig. 1.4

[3]

[Turn over

**2** Fig. 2.1 shows some of the cameras in a CCTV system. All of the cameras in the system are connected to a single video recorder by a cable The cable has a bandwidth of only 200 kHz.

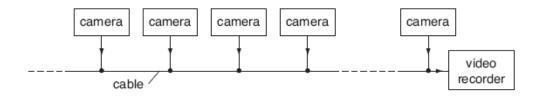


Fig. 2.1

(a)	The	cameras	use	time-division	multiplexing	to	send	their	images	in	digital	format	to	the
	vide	o recorde	r.											

(1)	explain the advantage of sending camera information in digital form rather than in analogue form.
	[3]
(ii)	Describe the process of time-division multiplexing.
	[23]

7

	·
(b)	Each camera scans 12 images every minute.
	Each image has 128 lines of pixels.
	There are 190 pixels in each line.
	The signal from each pixel is coded as five-bit word.
	By explaining the relationship between bandwidth and bit rate, use the information above to estimate the maximum number of cameras which can be connected to the cable.
	[8]

3 Fig. 3.1 shows the circuit of a five-bit analogue-to-digital converter.

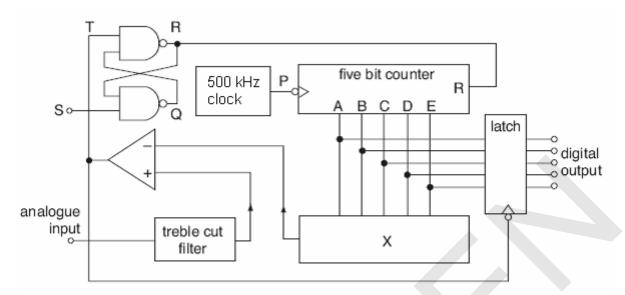
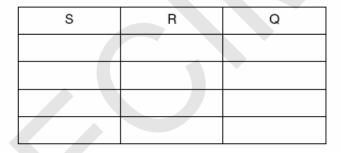


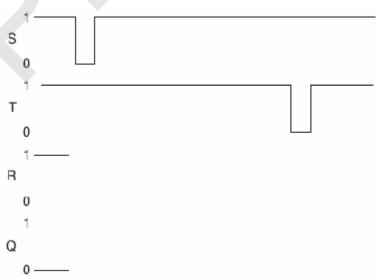
Fig. 3.1

- (a) Conversion of the analogue signal placed at the input starts when S is pulsed low. When conversion has taken place, the op-amp comparator pulses T low.
  - (i) Complete the truth table for a NAND gate with inputs S and R.



[3]

(ii) Complete the timing diagram of Fig. 3.2 for the signals leaving the NAND gate bistable.



(b)	Describe, in detail, the behaviour of the component labelled X in Fig. 3.1.
	FOI
	[3]
(c)	The filter at the analogue input of the converter has the gain-frequency graph shown in Fig. 3.3.
	1
	voltage 0.1
	gain 0.1
	0.01
	0.001
	0.05 0.5 5 50 500 frequency/kHz
	Fig. 3.3
	Complete Fig. 3.4 to show how the filter can be made from an op-amp and other
	components. Include component values and justify them with calculations.
	Fig. 3.4 [5]
(d)	Explain why a break frequency of 5 kHz is suitable for a clock frequency of 500 kHz.
	[4]
	[Turn over

**4** Fig. 4.1 shows the circuit diagram of the Schmitt trigger at the end of a cable carrying digital information in serial form.

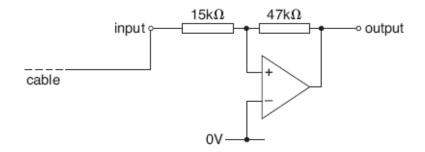


Fig. 4.1

(a) Explain why the component values set the trigger thresholds of the circuit at about ±4V.

[4]

(b) Fig. 4.1 shows a very noisy signal at the input of the Schmitt trigger.

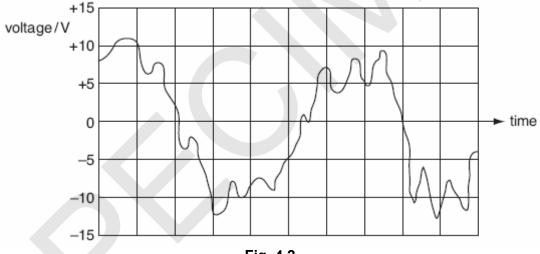


Fig. 4.2

Draw on Fig. 4.1 to show the signal at the output of the Schmitt trigger.

[3]

(c)	Explain the function of the Schmitt trigger at the end of the cable.
	10

(d)	Dat	a arrives along the cable as <b>packets</b> .
	(i)	Each packet has a start bit and a stop bit. Why are they necessary?
		[2]
	(ii)	Each packet is a 128-bit word which contains four different types of information. One of these is the data payload. Explain the need for the other three types of information.
		Test.
		[6]

**5** Fig. 5.1 is an incomplete block diagram for a superhet radio receiver.

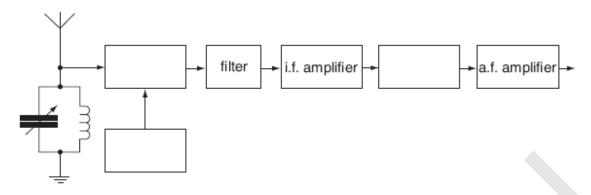


Fig. 5.1

(a)	Cor	nplete the blo	ock diagram. Choose na	mes for the blocks from the	following.	
		aerial	demodulator	local oscillator	mixer	
						[3]
(b)	The	filter blocks	out all signals, other tha	n those between 400 kHz to	600 kHz.	
	(i)	FM broadca	sts rather than AM ones		-	
	(ii)	How is an F	M broadcast different fro			
						. [3]
	(iii)		equency of the local os 92.0 MHz. Justify your ar	cillator when the receiver inswer.	s tuned to a broadca	st

frequency = ..... MHz **[2]** 

(iv)	Describe how the superhet receiver of Fig. 5.1 operates.
	[5]
Ex	Fig. 5.2  splain how the superhet receiver of Fig. 5.1 is an improvement on the simple receiver own in Fig. 5.2.
	e quality of your written communication will be assessed in this question.
	[8]

[Turn over

6 Fig. 6.1 shows a pulse-width modulator (PWM) based on a 50 kHz triangle wavefrom.

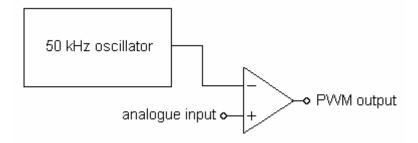


Fig. 6.1

(a) On the axes of Fig. 6.2, sketch the waveform for the PWM output for the analogue input shown.

[3]

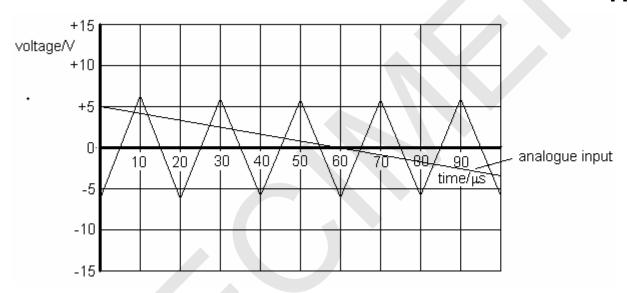


Fig. 6.2

**(b)** Fig. 6.3 shows a non-inverting Schmitt trigger with trip points at  $\pm$  6.5 V.

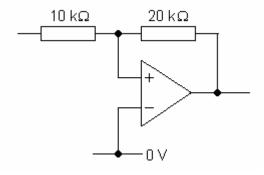
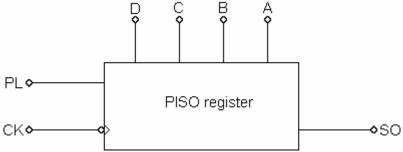


Fig. 6.3

On Fig. 6.3, show how the Schmitt trigger can be combined with a ramp generator to make a 50 kHz triangle waveform generator. Show all component values and justify them.

**7** Fig. 7.1 shows a parallel-in serial-out (PISO) shift register.



	CK <b>◇</b>	→\$SO
	Fig. 7.1	
(a)	Describe the behaviour of this PISO register.	
		[5]
(b)	In the space below, draw a circuit diagram to show how constructed from D flip-flops and logic gates. Explain how	w the register of Fig. 7.1 can be the circuit operates.
	The state of the s	,
		[6]
(c)	PISO registers in parallel-to-serial converters usually oscillators. Explain why.	use clock signals from crystal

[Paper Total: 110]

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### OXFORD CAMBRIDGE AND RSA EXAMINATIONS

**Advanced GCE** 

ELECTRONICS F615

Unit F615: Communications Systems

**Specimen Mark Scheme** 

The maximum mark for this paper is **110**.



Question Number	Answer	Max Mark				
1(a)(i)	440 kHz	[1]				
(ii)	sidebands are at 445 and 435 kHz idea of sidebands at carrier ± signal frequency	[3]				
(iii)	four divisions for 1 cycle of modulation $T = 1/5 \times 10^3 = 0.2$ ms or 200 $\mu$ s setting is 200 / 4 ( = 50 $\mu$ s/division)	[3]				
(b)(i)	diode in series resistor in parallel  modulated output  arrier  2nF					
	cv	[2]				
(ii)	allows r.f. components to be filtered out without affecting signal at 5 kHz	[2]				
(iii)	$R = 1/2\pi fC$ $R = 1/2\pi \times 30 \times 10^{3} \times 2 \times 10^{-9}$ $R = 2.7 \text{ k}\Omega$	[3]				
(iv)	sine wave of correct frequency correct amplitude correct bias					
		[3]				

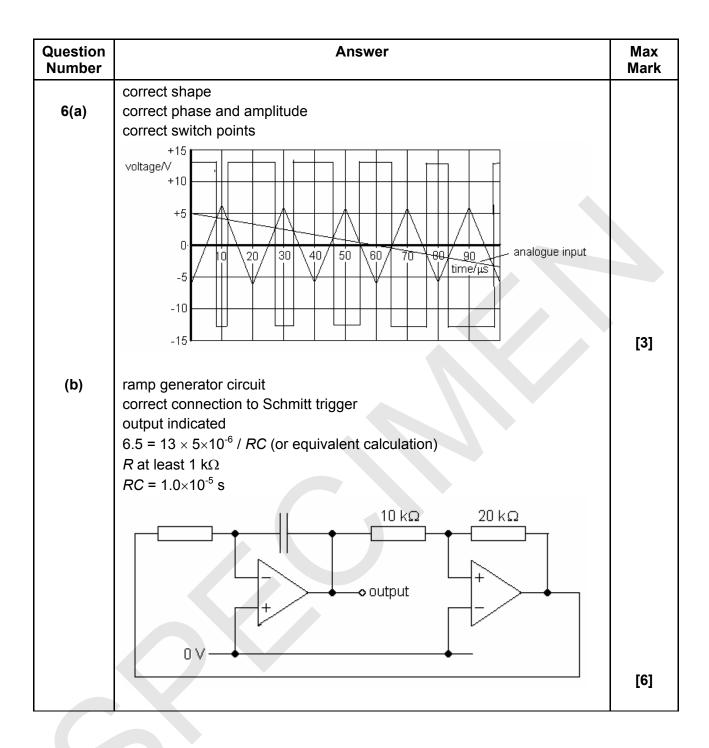
Question Number	Answer			
2(a)(i) (ii)	better quality / lower noise noise gained in transmission can be removed by limiters / Schmitt triggers  each signal is transmitted in bursts many times a second	[3]		
	in between data from other signals	[3]		
(b)	Stretch & Challenge, only award marks for fully correct answers.			
	bit rate - bandwidth relationship:  consider worst-case signal of 101010101  equivalent to a square wave signal  which can be transmitted as a sine wave  and regenerated at receiver by a limiter / Schmitt trigger  why cycles per second equal to half bits per second NOT just	[5]		
	quoting a rule estimate:  • bit rate for cable = $2 \times 200 \times 10^3 = 400\ 000\ \text{bps}$ • bit rate per camera = $5 \times 190 \times 128\ /\ 5 = 24\ 320\ \text{bps}$ • no ecf: cameras = $400\ 000\ /\ 24\ 320 = 16$	[3]		

Question Number	Answer	Max Mark	
3(a)(i)	all four different states of SR Q = 1 when S or R are low Q = 0 only when SR = 11		
	S R Q		
	0 0 1 0 0		
	1 0 1		
		[3]	
(ii)	R opposite of Q Q goes high on falling edge of S and returns high on falling edge of T	b	
		[2]	
(b)	outputs a voltage dependant on five-word input voltage proportional to binary value of word (owtte)	[3]	
(c)	correct circuit for inverting amplifier capacitor in parallel with feedback resistor all resistors at least 1 k $\Omega$ and not more than 1 M $\Omega$ $R_f/R_{in} = 0.1$ $R_fC = 3.2 \times 10^{-5}$ s	[5]	
(d)	each sample needs up to $2^5$ = 32 clock pulses taking a time of $32 \times (1/500 \times 10^3) = 64 \mu s$ maximum sample rate is $1/64 \times 10^{-6} = 16 \text{ kHz}$		
	which is at least double break frequency of 5 kHz (owtte)	[4]	

Question Number	Answer	Max Mark
4(a)	output saturates at +13V (or -13V) non-inverting input needs to go below 0 V to trip the circuit 13 V across 47 k $\Omega$ is 0.28 V per k $\Omega$ so 0.28 $\times$ 15 = 4.1 V across 15 k $\Omega$ ACCEPT alternative calculations involving current	[4]
(b)	correct shape saturating at ±13 V correct phase correct trip points (by eye)	[3]
(c)	restores signal to a digital one getting rid of noise added to the signal	[2]
(d)(i)	start bit alerts receiver that a packet is arriving stop bit restores line voltage to default so that next start bit can be detected (owtte)	[2]
(ii)	source address to identify system which placed the packet on the cable destination address to identify the system which needs to read the packet checksum	
	to identify/repair errors in transmission	[6]

Question Number	Answer				
5(a)	[1] per correct entry  mixer  filter  i.f. amplifier  dcmodulatcr  a.f. amplifier  oscillator				
	<del>-</del>	[3]			
(b)(i)	(200 kHz) bandwidth is large AM only needs twice maximum audio frequency ( $2 \times 20 = 40 \text{ kHz}$ )	[2]			
(ii)	(instantaneous) voltage of signal determines amplitude of an AM broadcast frequency of an FM broadcast	[3]			
(iii)	92.5 MHz filter centre-frequency is 0.5 MHz	[2]			
(iv)	<ul> <li>any of the following, maximum [5]</li> <li>mixer allows aerial signal to be modulated by oscillator</li> <li>generating copy of aerial signal at intermediate frequency</li> <li>filter removes anything on either side of intermediate frequency</li> <li>i.f. amplifier boosts amplitude of signal</li> <li>demodulator extracts a.f. signal from i.f. signal</li> <li>a.f. amplifier boosts amplitude / power of audio frequency signal</li> </ul>				
(c)	<ul> <li>any of the following, maximum [5]</li> <li>more selective</li> <li>superhet filter has sharp edges (owtte)</li> <li>to remove neighbouring broadcasts</li> <li>more sensitive</li> <li>superhet has amplification before demodulation</li> <li>so that weaker broadcasts can be heard</li> </ul>				

Question Number	Answer			
5(c) cont'd	Qualit	y of Written Communication is assessed in this question		
Cont u	3	The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.		
	2	The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.		
	1	The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.	<b>701</b>	
	0	The language has no rewardable features.	[8]	



Question Number	Answer		
7(a)	when PL pulsed high/low word at DCBA is read in with A appearing at SO falling edges at CK replaces A with B, C and D in turn	[5]	
(b)	Stretch & Challenge, only award marks for fully correct answers.  Design must be compatible with description of (a).  circuit diagram:  four D flip-flops with clock lines in parallel  with series NOT gate to input CK  Q to D of next flip-flop, last Q labelled SO  correct use of S and R and gates / multiplexers for parallel loading	[4]	
	<ul> <li>explanation</li> <li>operation of parallel loading circuitry in terms of behaviour of gates / multiplexers</li> <li>operation of serial output in terms of behaviour of D flip-flops</li> <li>e.g.</li> </ul>	[2]	
(c)	very stable frequency same oscillator can be used in receiver	[2]	
	Paper Total	[110]	

## Assessment Objectives Grid (includes QWC)

Question	AO1	AO2	AO3	Total	Synoptic
1(a)(i)		1		1	
1(a)(ii)	1	2		3	
1(a)(iii)	1	2		3	
1(b)(i)	1	1		2	
1(b)(ii)	1	1		2	
1(b)(iii)	1	2		3	3
1(b)(iv)	1	2		3	
2(a)(i)	1	2		3	
2(a)(ii)	1	2		3	
2(b)	2	6		8	
3(a)(i)	3			3	3
3(a)(ii)		2		2	2
3(b)	1	2		3	
3(c)	2	3		5	5
3(d)	1	3		4	7
4(a)		4		4	
4(b)		3		3	
4(c)	2			2	
4(d)(i)	2			2	
4(d)(ii)	3	3		6	
5(a)	3			3	
5(b)(i)	1	1		2	
5(b)(ii)	1	2		3	
5(b)(iii)	1	1		2	
5(b)(iv)	3	2		5	
5(d)	4	4		8	
6(a)		3		3	3
6(b)	3	3		6	4
7(a)	2	3		5	
7(b)	2	4		6	
7(c)	2			2	
Totals	46	64	0	110	20