

OXFORD CAMBRIDGE AND RSA EXAMINATIONS
LEVEL 1/2
R113/01
CAMBRIDGE NATIONAL IN SYSTEMS
CONTROL IN ENGINEERING
Electronic principles

WEDNESDAY 13 JANUARY 2016: Afternoon

DURATION: 1 hour
plus your additional time allowance

MODIFIED ENLARGED

Candidate forename		Candidate surname	
-------------------------------	--	------------------------------	--

Centre number						Candidate number				
--------------------------	--	--	--	--	--	-----------------------------	--	--	--	--

Candidates answer on the Question Paper.

OCR SUPPLIED MATERIALS:

None

OTHER MATERIALS REQUIRED:

A calculator may be used

READ INSTRUCTIONS OVERLEAF

INSTRUCTIONS TO CANDIDATES

Use black ink. HB pencil may be used for graphs and diagrams only.

Complete the boxes on the first page with your name, centre number and candidate number.

Answer ALL the questions.

Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your candidate number, centre number and question number(s).

INFORMATION FOR CANDIDATES

The total number of marks for this paper is 60.

The number of marks for each question is given in brackets [] at the end of the question or part question.

Dimensions are in millimetres unless stated otherwise.

Your quality of written communication will be assessed in questions marked with an asterisk(*).

Any blank pages are indicated.

BLANK PAGE

Answer ALL questions.

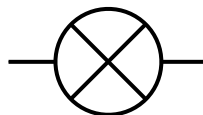
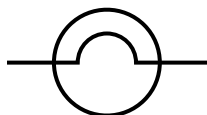
- 1 (a) Complete the table by naming the unit for each quantity shown.**

QUANTITY	UNIT
Capacitance	
Frequency	

[2]

- (b) Name the two component symbols shown in Fig. 1.**

Fig. 1



[2]

- (c) A resistor has a current flowing through it of 10 A and a voltage across it of 220V.**

Calculate:

- (i) the value of the resistor in ohms**

_____ [2]

- (ii) the power, in watts, absorbed by the resistor.**

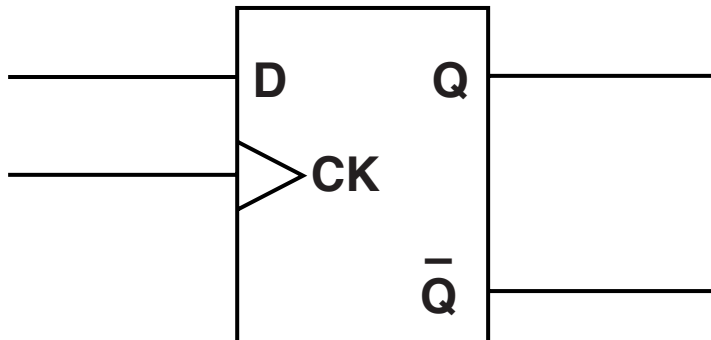
_____ [2]

- (d) Determine the total resistance of a circuit made up of two resistors in series of value $18\ \Omega$ and $22\ \Omega$.**

_____ [2]

- 2 Fig. 2 shows a D type bistable with a positive edge trigger.

Fig. 2



- (a) State the meaning of each of the connections.

Terminal D _____

Terminal CK _____

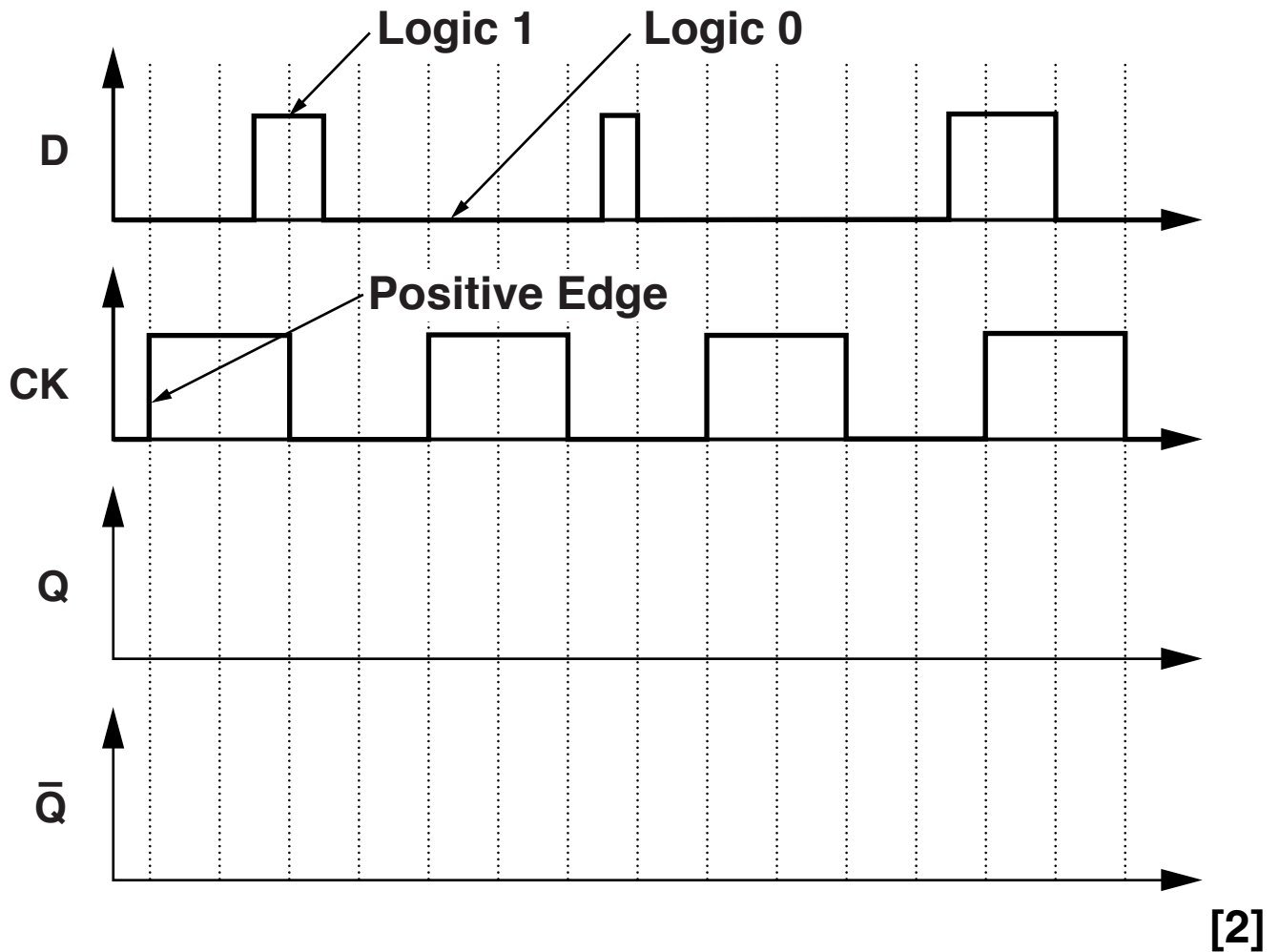
Terminal Q _____

Terminal \bar{Q} _____

[4]

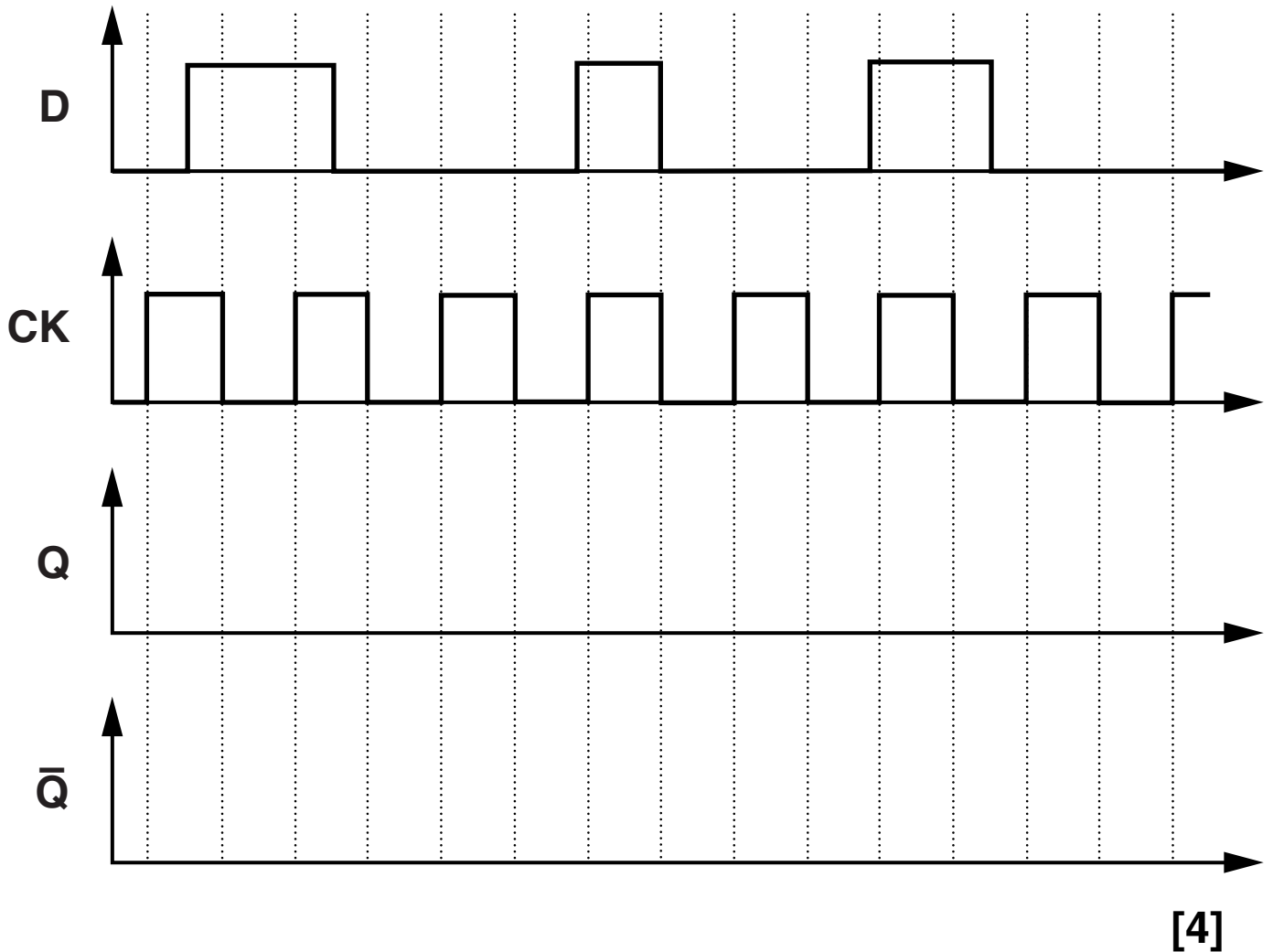
(b) Complete the timing diagrams for a positive edge-triggered D type bistable shown in Fig. 3.

Fig. 3



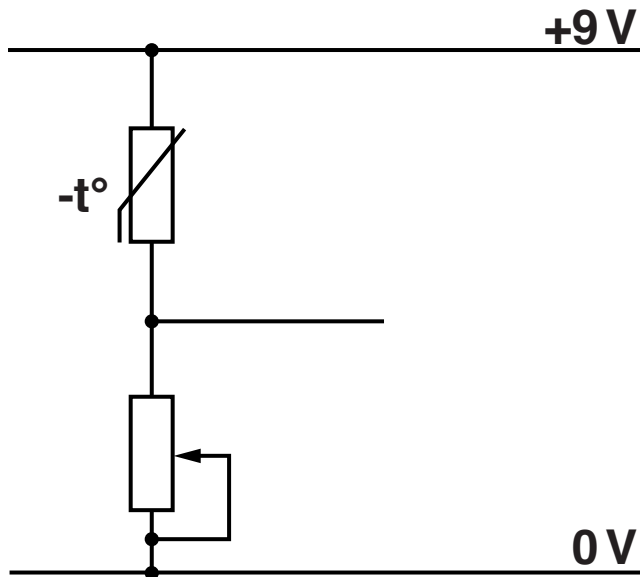
(c) For a different situation, complete the timing diagrams for a positive edge-triggered D type bistable shown in Fig. 4.

Fig. 4



- 3 Fig. 5 shows part of a potential divider circuit using an NTC thermistor.


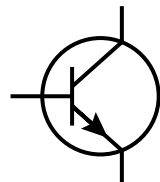
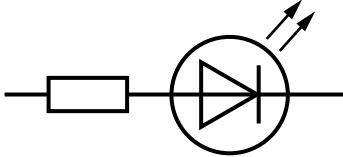
Fig. 5



- (a) Label the diagram in Fig. 5 to identify the NTC thermistor.

[1]

- (b) Complete the circuit diagram in Fig. 5 by adding the symbols shown in the table below. [3]

COMPONENT	SYMBOL
base resistor	
npn transistor	
LED with a protective resistor	

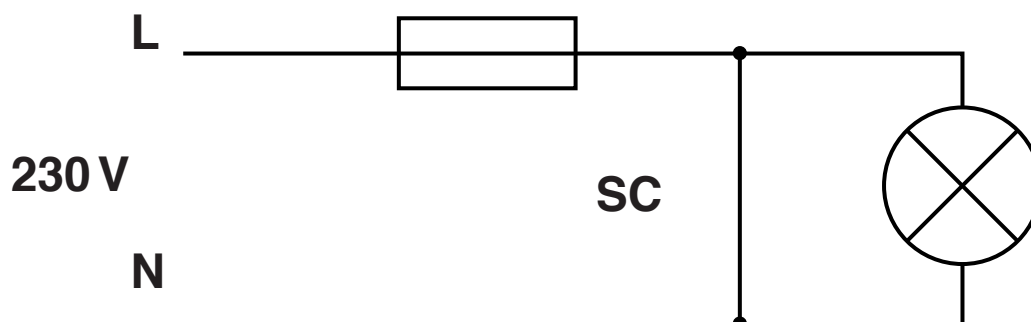
- (c) Label the transistor with the terms emitter(e), collector(c) and base(b). [1]

- (d) Explain in detail how the circuit works.

[5]

- 4 Fig. 6 shows a lighting circuit which has been short circuited (SC) between the live and neutral wires.

Fig. 6

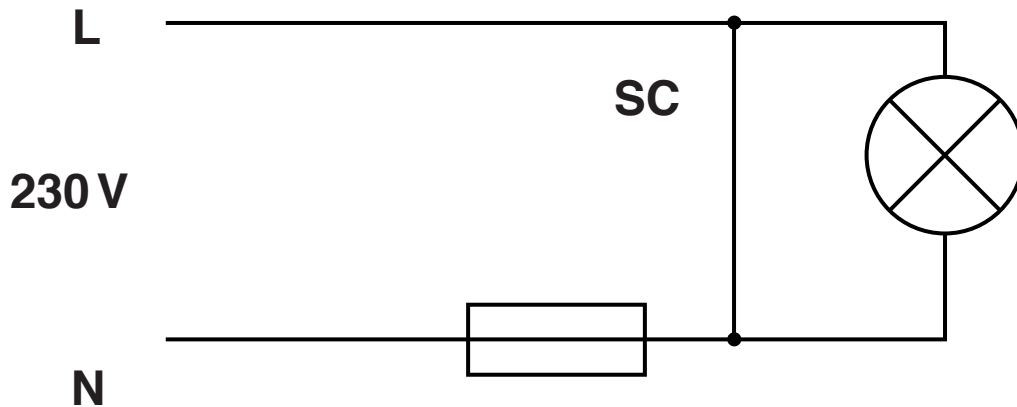


- (a) Explain why the circuit is not in a dangerous condition when the fuse blows.

[2]

(b) Fig. 7 now shows the fuse in a different position and again short circuited.

Fig. 7

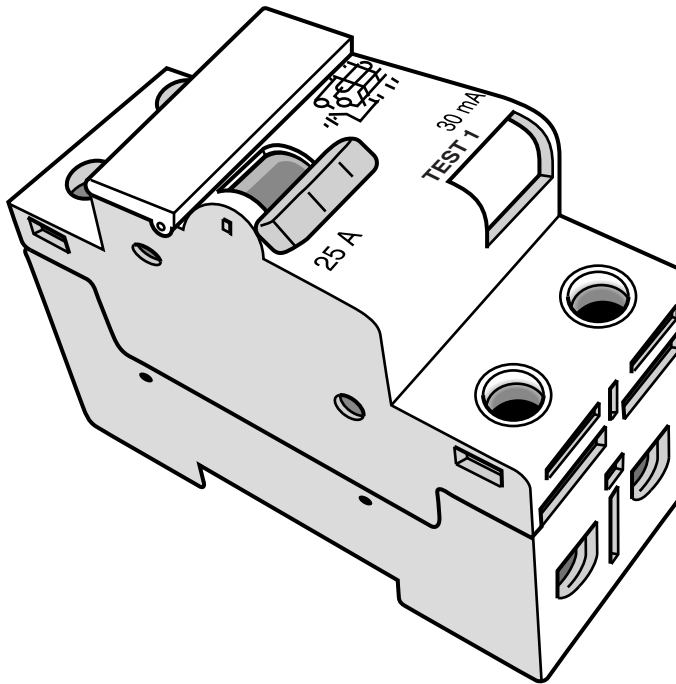


Explain why the circuit is still dangerous even though the fuse has blown.

[3]

- (c) Fig. 8 shows a device that is used to prevent danger if there is a problem in an electrical circuit.

Fig. 8



- (i) Name the device shown in Fig. 8.

_____ [1]

- (ii) Explain how the device works.

_____ [4]

- 5 (a) Complete the truth table shown below for a two-input AND, OR and NOR gate.

Input A	Input B	AND gate output	OR gate output	NOR gate output
0	0			
0	1			
1	0			
1	1			

[3]

- (b) Explain what is meant by the terms logic level 1 and logic level 0 when used with logic gates.

logic level 1 _____

logic level 0 _____

_____ [2]

(c) Draw a diagram to show how a two-input NAND gate can be used as a NOT gate.

[2]

(d) State the main characteristics of an exclusive-OR gate (XOR).

[3]

- 6 (a) Describe a quality assurance method used during commercial printed circuit board production including the finished product.**

[4]

- (b)* Discuss the benefits and drawbacks to the manufacturer of using 'surface mount' technology compared to 'through hole' technology when manufacturing circuits.**

[6]

[illegible]

END OF QUESTION PAPER

BLANK PAGE

BLANK PAGE

Copyright Information

OCR is committed to seeking permission to reproduce all third-party content that it uses in its assessment materials. OCR has attempted to identify and contact all copyright holders whose work is used in this paper. To avoid the issue of disclosure of answer-related information to candidates, all copyright acknowledgements are reproduced in the OCR Copyright Acknowledgements Booklet. This is produced for each series of examinations and is freely available to download from our public website (www.ocr.org.uk) after the live examination series.

If OCR has unwittingly failed to correctly acknowledge or clear any third-party content in this assessment material, OCR will be happy to correct its mistake at the earliest possible opportunity.

For queries or further information please contact the Copyright Team, First Floor, 9 Hills Road, Cambridge CB2 1GE.

OCR is part of the Cambridge Assessment Group; Cambridge Assessment is the brand name of University of Cambridge Local Examinations Syndicate (UCLES), which is itself a department of the University of Cambridge.

